



TangerineSDR



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RF Module (RFM)

Requirements Document

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1. INTRODUCTION.....	4
1.1. Cost Goals.....	4
1.2. References	4
1.3. Form Factor Objective	4
2. POWER SUPPLY	5
3. RF MODULE INPUTS AND OUTPUTS.....	5
4. RF MODULE PERFORMANCE REQUIREMENTS.....	6
4.1. Receiver Noise Figure	6
4.2. Dynamic Range.....	6
4.3. ADC Clock Input	6
4.4. Clock Input Phase Noise.....	7
4.5. Noise Source and Control.....	7
4.6. Attenuator and Control	8
4.7. Filter Module	8
5. MODULE VARIANTS	8

1. Introduction

The Tangerine SDR Receiver Module receives radio frequency signals in the 100 kHz to 30 MHz range, optionally filters and attenuates the signals, digitizes the signals with a low-jitter clock, and transfers the digitized samples to the Tangerine SDR Data Engine module.

The module also contains an integrated noise source that can programmatically connect the receiver input to a known level of broadband noise used to calibrate the receiver sensitivity. The noise signal is injected ahead of the attenuator and filter. This provides the ability to capture test data that will allow determination of filter and other characteristics being applied to the received RF signal.

For the Personal Space Weather Station (PSWS) the Dual-channel variant will be used. The dual-channel receiver contains two complete receivers, from the antenna connector through the ADC. The dual channel unit can optionally share a single noise calibration source, but will require two relays to select the noise source. It will also contain two plug in RF filters, two programmable attenuators, etc.

1.1. *Cost Goals*

The cost goal of the Dual Channel RF module is \$TBD. No cost goal is established for the Single channel variant at this time.

1.2. *References*

- The RF module detailed form factor, mechanical layout, electrical signal interconnection, connectors and pinouts, and electrical specifications are described in the Interface Control Document (ICD) for the RF module.
- Tangerine SDR Clock Module Specification. Sets the jitter, frequency accuracy, channel-to-channel coherence and phase noise of the clock inputs to the RF Module.
- Single and Dual channel ADC and ADC driver integrated circuit manufacturer data sheets.

1.3. *Form Factor Objective*

The form factor will be defined in the ICD document for the RF Modules.

Discussion (for further study):

The Dual channel module is planned to fit in the RFM single module size identified in the drawing, and is 40mm wide by TBD mm in length. An M.2 connector is on one 40mm side and two SMA connectors on the opposite 40mm side.

The anticipated module density is very tight for the dual-channel unit. Another option may be to use a dual-M.2 module of dimensions roughly 85 mm by TBD mm. This would eliminate the ability to equip the second RFM slot with a transmitter module, but a transmitter module may not be needed in the PSWS application.

The single channel RF module might fit in the single RM module outline, allowing a transmitter module to occupy the other RF Module slot.

2. Power Supply

The RF Module shall be powered from:

- +3.3 VDC, and shall draw less than TBD mA.
- +5VDC, and shall draw less than TBD mA.
- +12 VDC at 10 mA may be needed for the noise source. If the noise source can be redesigned to operate at +5 VDC, then this supply can be eliminated.

3. RF Module Inputs and Outputs

The RF module is connected to the Data Engine via an M.2 connector. This connection provides power, clocks, noise source control line, and attenuator control to the RF module (inputs) and generates output data samples to the Data Engine.

The connection to the receive antenna is via two SMA receptacles (one per channel) on the module.

The RF module ADC clock must meet a tight jitter requirement in order to allow the ADC to meet the sensitivity requirement at higher RF frequencies (30 MHz). See the clock module specification.

In the case of the dual channel RF modules, the two channels must be clocked by phase-coherent ADC sample clocks. It is recommended that the dual channel unit use signals for the ADC clocks for the two ADC converters that are referenceable to a single common clock in order to maintain tight phase coherence between the two channels. If the ADC clocks between the two channels were to vary with respect to one another, the downconverted baseband phase between them would wander causing the loss of ability to use the two channels for receive polarization control.

While two receive antennas plus the interconnecting cables will have different delays, those are static and can be removed via a one-time calibration. However if the ADC clocks drift relative to one another the resultant phase delay cannot be removed via prior calibration.

The module shall provide an ADC overload output signal for each ADC indicating that the ADC has exceeded its digitization range.

4. RF Module Performance Requirements

The RF module shall meet the following requirements:

4.1. Receiver Noise Figure

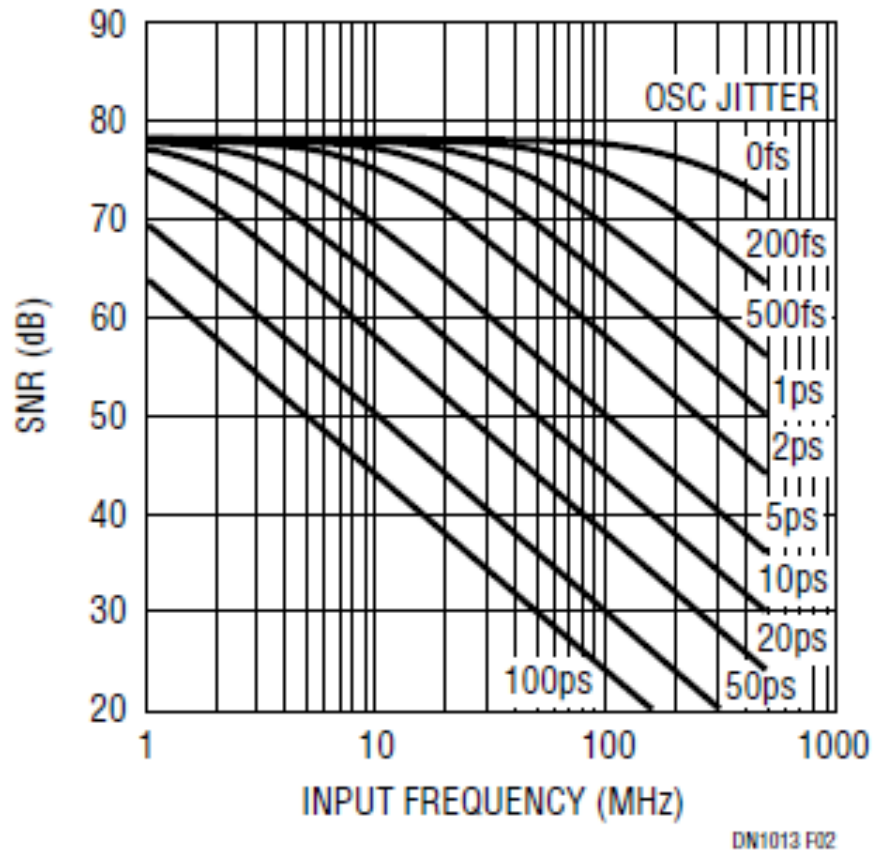
The RF module at minimum attenuator setting, and with the filter bypassed shall achieve a Noise Figure of TBD dB across the 100 kHz to 30 MHz range. Note: The Noise Figure is likely to be about 6.5 dB. However the requirement does not need to be this low because the manmade noise level across most of the HF frequency range will be higher. 10 dB or less is probably reasonable, but the requirement is TBD until characterization is completed. If the NF climbs much above 10 dB then noise calibration becomes more difficult as the Excess Noise Ratio (ENR) of the noise source will have to be increased.

4.2. Dynamic Range

The dynamic range of the receiver shall be specified as the ratio of peak signal to either spurious ADC artifacts, or to 3rd order intermodulation products after the signal has been decimated to bring the ADC noise floor below the spurious products. The objective dynamic range is 88 dB or greater for both ADC spurious and receiver intermodulation products.

4.3. ADC Clock Input

The ADC clock shall exhibit less than ± 1 picoseconds jitter, peak. Note: Jitter on this clock degrades the SNR of the ADC conversion. See figure below from a representative ADC specification which graphs this effect. The ADC clock jitter is determined by the Clock Module and its specification.



4.4. Clock Input Phase Noise

The ADC clock input to the RF module shall meet the Phase Noise requirements in the Clock Module specification. Briefly these are:

- The clock and synthesizer phase noise shall be less than -60 dBc at 1 Hz offset, declining as 1/f to less than -120 dBc at 1 kHz offset.
- The phase noise is specified at the NCO frequency of 30 MHz. The NCO is the internal FPGA quadrature down-conversion oscillator. (Since this point is inaccessible, the specification shall be verified by measurement of the resultant baseband signal).

4.5. Noise Source and Control

Preliminary: The noise source will provide an Excess Noise Ratio (ENR) of 10.0 dB from 100 kHz to 30 MHz. It may be necessary to adjust the ENR specification to assure that

the noise is above the ADC noise level sufficiently. The specification is preliminary until characterization is done.

The RF module shall provide an input binary signal to turn the noise source on and off. When the noise source is OFF, a relay will select the normal receive signal from the RF input connector. When the noise source is ON the relay will connect instead to the noise source. It is desirable to have the relay function ahead of the attenuator and plug-on filter. This allows using the noise source to verify the attenuator and filter module settings.

For the dual channel unit, a single control bit may be used to switch the noise selection relay for both receivers.

4.6. Attenuator and Control

The receiver shall implement a programmable attenuator from 0 dB to 31 dB in 1 dB steps. The attenuator control signals select the value of attenuation. These signals are in a 5-bit parallel binary word format. One attenuator per channel is required. On the dual channel receiver the two attenuators shall be independently settable.

4.7. Filter Module

The receiver will be fitted with a socket on which to plug an optional filter module. The socket can be bypassed if no filter is used. The purpose of the filter is to remove undesired strong signals that would otherwise overload the ADC or degrade the dynamic range of the receiver. For example, an AM Broadcast Band Reject filter may be needed in some locations to prevent ADC overload. Similarly some locations may require a Shortwave reject filter, or an FM/TV Broadcast lowpass filter. One filter module socket per channel shall be provided.

5. Module Variants

The RF Module will have multiple variants optimized for different functions. This specification is written specifically around the dual-channel variant. The single channel variant will be lower cost, and the specification can easily be interpreted for that variant.

Module Variant	Physical Form	Key Use	Key Differences
Dual Channel	Single RF Module, single M.2 connector. 2 RF SMA connectors.	PSWS	Dual channel ADC with common ADC clock, 2 RF connectors, 2 filters, 2 attenuators, 2 noise relays.
Single Channel	Single RF Module, single M.2 connector, 1 RF SMA connector.	Low cost non-PSWS applications.	Single RF channel and attendant functions.

