TangerineSDR

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Clock Module (CKM)

Interface Control Document

Version Number: 0.2.1

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VERSION HISTORY

Version Number	Implemented By	Revision Date	Approved By	Approval Date	Description of Change
0.1	T. McDermott	July 10, 2019			Original Issue.
0.2	T. McDermott	July 12, 2019			Separate out GPS antenna and Ext Clock Ref. to separate connectors J1, J2 (SMA).
0.2.1	T. McDermott	August 1, 2019			Reformat and Change Document Number

1. Introduction

The Personal Space Weather Station (PSWS) Clock Module provides GPS derived time and frequency for input to the PSWS TangerineSDR receiver Data Engine (DE). It is a low cost module that provides a high accuracy pulse-per-second (PPS) timing strobe, high-accuracy UTC time, and programmable frequency synthesizer outputs derived from a GPS disciplined oscillator. The four synthesizer outputs have phase noise performance that meets the needs of the PSWS receiver. The module is intended to be programmed from the DE, and to provide timing and frequency signals to the DE. Figure 1 is a block diagram of the Clock Module.

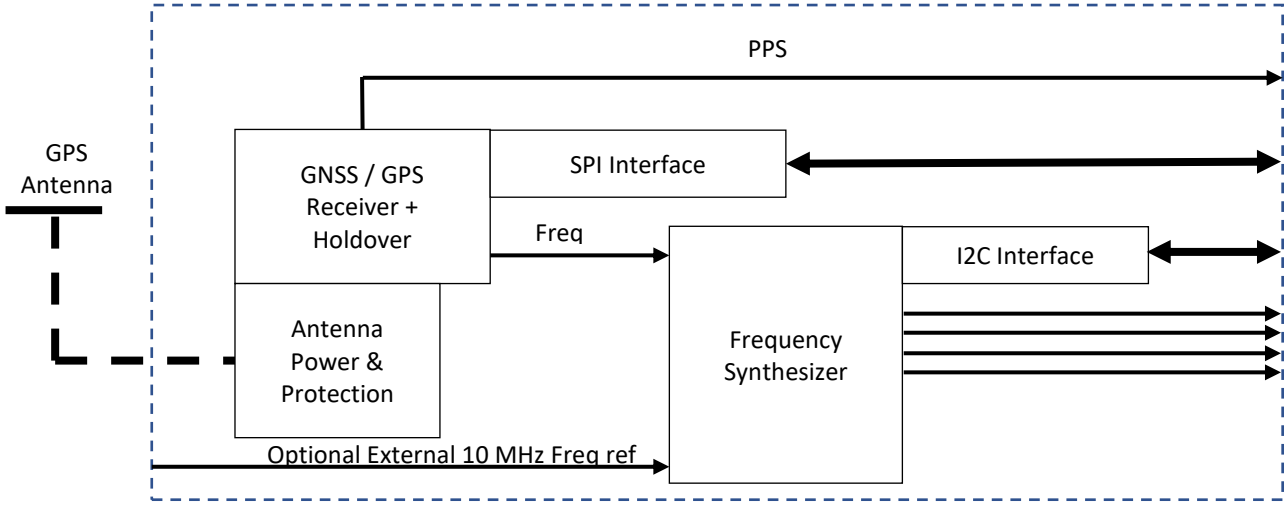

Figure 1. Block Diagram of Clock Module

The clock module contains a holdover oscillator which continues the phase and frequency outputs when GPS receiver signal is lost. It uses a low-phase-noise oscillator with frequency stability correction. The holdover oscillator may be integrated within the GPS receiver, or it may be outside the receiver but contained on the module.

1.1. References

The PSWS Clock Module Specification describes the purpose, use cases, functionality and performance requirements for the clock module.

1.2. GPS Receiver

The GPS receiver registers, block diagrams, and control / status maps are available from the manufacturer programming document. While the exact GPS module choice is still TBD, a representative module would be the u-blox LEA-M8F.

- All Documentation located at:

https://www.u-blox.com/en/product/lea-m8f-module#tab-documentation-resources

- Datasheet: UBX-14001772
- Hardware Integration Manual: UBX-14000034
- System Integration Guide: UBX-14001603
- Receiver Description + Protocol Specification: UBX-13003221

1.3. Synthesizer

The Synthesizer registers, block diagrams, and control / status maps are available from the manufacturer programming document. While the exact Synthesizer choice is still TBD, a representative choice would be the Silicon Labs SI-5344 D.

- The documentation is not centrally collected, individual links are needed.
- Evaluation Board User's Guide: https://www.silabs.com/documents/public/user-guides/Si5344-D-EVB.pdf
- Datasheet: https://www.silabs.com/documents/public/data-sheets/Si5345-44-42-D-DataSheet.pdf
- Reference Manual: https://www.silabs.com/documents/public/reference-manuals/Si5345-44-42-D-RM.pdf

2. Electrical Interfaces

This section defines the electrical interfaces of the Clock Module, including the connectors, connector pin outs, signals, and signal formats. Control signals are contained on a single M.2 connector. GPS and External Ref Clock signals are on SMA connectors. The module has two intended uses:

1. Plug onto a Tangerine SDR Data Engine board using the M.2 connector.
2. Independent use by plugging onto a breakout board which routes the M.2 connector to various connectors for SPI, I2C, and Synthesizer outputs.

J1 - GPS Receive Antenna + DC Power to Antenna Connector type: SMA Receptacle				
Connector Pin #	**Signal Name**	**Signal Electrical Format**	**Input / Output / Bidirectional**	**Description**
1	GPS Antenna	50 ohm RF Coaxial also supplying power	B	Output - Provides current-limited DC power (+3.3VDC or +5VDC TBD) to the GPS antenna. Input – receives the 1.5 GHz GPS signal from the antenna.

J2 – External 10 MHz Reference Clock Input Connector type: SMA Receptacle				
Connector Pin #	**Signal Name**	**Signal Electrical Format**	**Input / Output / Bidirectional**	**Description**
1	External 10 MHz Reference	50 ohm RF Coaxial	I	Input – Receives Optional External 10 MHz reference inputs. Terminated 50 ohms.

J3 – GPS and Synthesizer Control and Status, PPS and Synthesizer Outputs Connector type: M.2 – xx-Keyed (B key ? or M key ?)				
Note the Pins numbers are WRONG and arbitrary at this time. The Exact pin layout will need to await the ICD for the Data Engine and analysis to prevent module interchangeability and potential power mis-supply problems.				
Connector Pin #	**Signal Name**	**Signal Electrical Format**	**Input / Output / Bidirectional**	**Description**
1	PPS+	LVDS	O	GPS Pulse Per Second differential positive
2	PPS-	LVDS	O	GPS Pulse Per Second differential negative
3	GND			
				GPS Receiver Control and Status (SPI)
4	SPI	3V CMOS	I	SCLK
5	SPI	3V CMOS	I	MOSI
6	SPI	3V CMOS	O	MISO
7	SPI	3V CMOS	I	SS
8	GND			
				Synthesizer Control and Status (I2C)
9	I2C	3V CMOS	B	SDA
10	I2C	3V CMOS	I	SCL
11	GND			
				Synthesizer Outputs
12	Syn1+	LVDS	O	Synthesizer 1 Positive
13	Syn1-	LVDS	O	Synthesizer 1 Negative
14	GND			
15	Syn2+	LVDS	O	Synthesizer 2 Positive
16	Syn2-	LVDS	O	Synthesizer 2 Negative
17	GND			
18	Syn3+	LVDS	O	Synthesizer 3 Positive
19	Syn3-	LVDS	O	Synthesizer 3 Negative
20	GND			
21	Syn4+	LVDS	O	Synthesizer 4 Positive
22	Syn4-	LVDS	O	Synthesizer 4 Negative
23	GND			

				Status Outputs (RESERVED if necessary to clock some time critical function in the FPGA)
24	Status 1+	LVDS	O	Output – Status 1 Positive (function TBD)
25	Status 1-	LVDS	O	Output – Status 1 Negative
26	GND			
27	Status 2+	LVDS	O	Output – Status 2 Positive (Function TBD)
28	Status 2-	LVDS	O	Output – Status 2 Negative
29	GND			
				DC Power
30, 31	+3.3	Power	I	+3.3 VDC Power. Current TBD
32, 33	+5	Power	I	+ 5 VDC Power. Current TBD.
34	GND			
TBD	M.2 CONNECTOR KEY			

3. Mechanical Interfaces

This section describes the mechanical packaging of the clock module, including board profile, mounting and screw holes, and connector placement.

The module profile is shown in Figure 3.1. TBD. The module dimensions are TBD.

The Main electrical connector type is TBD (might be M.2?). The module mounts to the PSWS Data Engine as shown in figure 3.2 using a TBD screw at the locations shown in the profile drawing.