TangerineSDR

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Clock Module (CKM)

Interface Control Document

Version Number: 0.3

Version Date: August 13, 2019

Document Number: TSDR-CKM-ICD

VERSION HISTORY

Version Number	Implemented By	Revision Date	Approved By	Approval Date	Description of Change
0.1	T. McDermott	July 10, 2019			Original Issue.
0.2	T. McDermott	July 12, 2019			Separate out GPS antenna and Ext Clock Ref. to separate connectors J1, J2 (SMA).
0.2.1	T. McDermott	August 1, 2019			Reformat and Change Document Number
0.3	T. McDermott	August 13, 2019			Change/add pins on M.2 connector J3. Reformat J3 table.

1. Introduction

The Personal Space Weather Station (PSWS) Clock Module provides GPS derived time and frequency for input to the PSWS TangerineSDR receiver Data Engine (DE). It is a low cost module that provides a high accuracy pulse-per-second (PPS) timing strobe, high-accuracy UTC time, and programmable frequency synthesizer outputs derived from a GPS disciplined oscillator. The four synthesizer outputs have phase noise performance that meets the needs of the PSWS receiver. The module is intended to be programmed from the DE, and to provide timing and frequency signals to the DE. Figure 1 is a block diagram of the Clock Module.

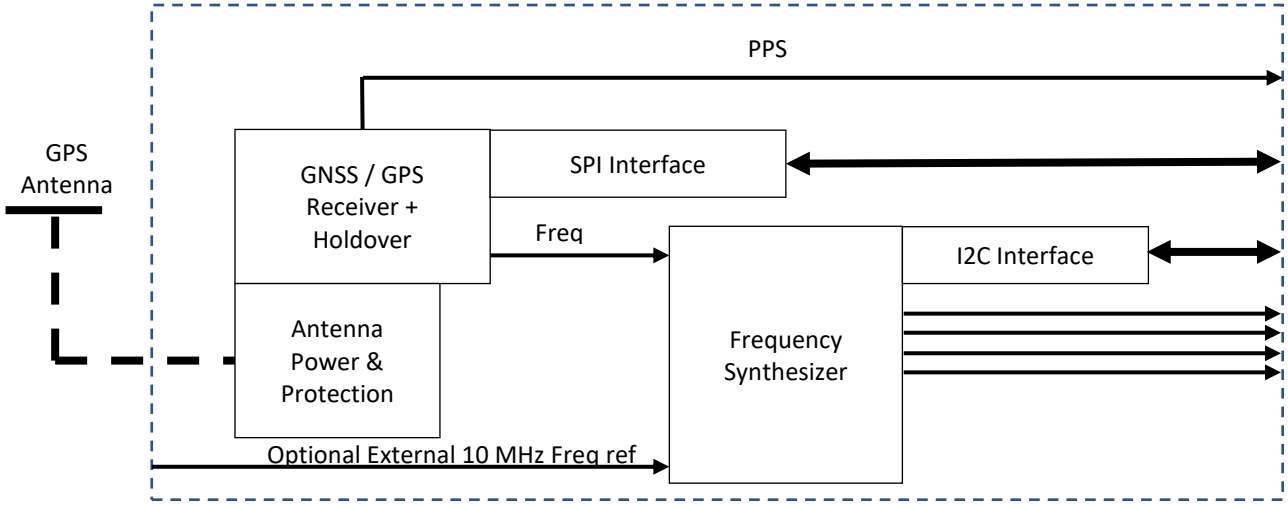

Figure 1. Block Diagram of Clock Module

The clock module contains a holdover oscillator which continues the phase and frequency outputs when GPS receiver signal is lost. It uses a low-phase-noise oscillator with frequency stability correction. The holdover oscillator may be integrated within the GPS receiver, or it may be outside the receiver but contained on the module.

1.1. References

The PSWS Clock Module Specification describes the purpose, use cases, functionality and performance requirements for the clock module.

1.2. GPS Receiver

The GPS receiver registers, block diagrams, and control / status maps are available from the manufacturer programming document. While the exact GPS module choice is still TBD, a representative module would be the u-blox LEA-M8F.

- All Documentation located at:

https://www.u-blox.com/en/product/lea-m8f-module#tab-documentation-resources

- Datasheet: UBX-14001772
- Hardware Integration Manual: UBX-14000034
- System Integration Guide: UBX-14001603
- Receiver Description + Protocol Specification: UBX-13003221

1.3. Synthesizer

The Synthesizer registers, block diagrams, and control / status maps are available from the manufacturer programming document. While the exact Synthesizer choice is still TBD, a representative choice would be the Silicon Labs SI-5344 D.

- The documentation is not centrally collected, individual links are needed.
- Evaluation Board User's Guide: https://www.silabs.com/documents/public/user-guides/Si5344-D-EVB.pdf
- Datasheet: https://www.silabs.com/documents/public/data-sheets/Si5345-44-42-D-DataSheet.pdf
- Reference Manual: https://www.silabs.com/documents/public/reference-manuals/Si5345-44-42-D-RM.pdf

2. Electrical Interfaces

This section defines the electrical interfaces of the Clock Module, including the connectors, connector pin outs, signals, and signal formats. Control signals are contained on a single M.2 connector. GPS and External Ref Clock signals are on SMA connectors. The module has two intended uses:

1. Plug onto a Tangerine SDR Data Engine board using the M.2 connector.
2. Independent use by plugging onto a breakout board which routes the M.2 connector to various connectors for SPI, I2C, and Synthesizer outputs.

J1 - GPS Receive Antenna + DC Power to Antenna Connector type: SMA Receptacle				
Connector Pin #	**Signal Name**	**Signal Electrical Format**	**Input / Output / Bidirectional**	**Description**
1	GPS Antenna	50 ohm RF Coaxial also supplying power	B	Output - Provides current-limited DC power (+3.3VDC or +5VDC TBD) to the GPS antenna. Input – receives the 1.5 GHz GPS signal from the antenna.

J2 – External 10 MHz Reference Clock Input Connector type: SMA Receptacle				
Connector Pin #	**Signal Name**	**Signal Electrical Format**	**Input / Output / Bidirectional**	**Description**
1	External 10 MHz Reference	50 ohm RF Coaxial	I	Input – Receives Optional External 10 MHz reference inputs. Terminated 50 ohms.

J3 – GPS and Synthesizer Control and Status, PPS and Synthesizer Outputs
Connector type: M.2 – M-Keyed

Note the Pins numbers are WRONG and arbitrary at this time.
The Exact pin layout will need to await the ICD for the Data Engine and analysis to prevent module interchangeability and potential power mis-supply problems.

NAME	LVL	DIR	Pin #	Pin #	DIR	LVL	Name
GND	PWR		1	2	I	3.3V CMOS	IDENT_I2C_CLK
CLKM_PPS_OUT+	LVDS	I	3	4	I/O	3.3V CMOS	IDENT_I2C_DAT
CLKM_PPS_OUT-	LVDS	I	5	6	I	3.3V CMOS	SPI_MOSI
GND	PWR		7	8	O	3.3V CMOS	SPI_MISO
SYN_I2C_CLK	3.3V CMOS	I	9	10	I	3.3V CMOS	SPI_CLK
SYN_I2C_DAT	3.3V CMOS	I	11	12	I	3.3V CMOS	SPI_SS
SYN_I2C_CS0n	3.3V CMOS	I	13	14	I	3.3V CMOS	Unused_I2C_CS1n
GND	PWR		15	16		PWR	GND
CLKM_SYN_OUT0+	LVDS	O	17	18	I	LVDS	Unused_CLKM_SYN_IN0+
CLKM_SYN_OUT0-	LVDS	O	19	20	I	LVDS	Unused_CLKM_SYN_IN0-
GND	PWR		21	22		PWR	GND
CLKM_SYN_OUT1+	LVDS	O	23	24	I	LVDS	Unused_CLKM_SYN_IN1+
CLKM_SYN_OUT1-	LVDS	O	25	26	I	LVDS	Unused_CLKM_SYN_IN1-
GND	PWR		27	28		PWR	GND
CLKM_SYN_OUT2+	LVDS	O	29	30	I	LVDS	Unused_CLKM_SYN_IN2+
CLKM_SYN_OUT2-	LVDS	O	31	32	I	LVDS	Unused_CLKM_SYN_IN2-
GND	PWR		33	34		PWR	GND
CLKM_SYN_OUT3+	LVDS	O	35	36	I	LVDS	Unused_CLKM_SYN_IN3+
CLKM_SYN_OUT3-	LVDS	O	37	38	I	LVDS	Unused_CLKM_SYN_IN3-
GND	PWR		39	40		PWR	GND
CLKM_STAT_OUT0+	LVDS	O	41	42	O	LVDS	CLKM_STAT_OUT1+
CLKM_STAT_OUT0-	LVDS	O	43	44	O	LVDS	CLKM_STAT_OUT1+
GND	PWR		45	46		PWR	GND
1.8V	PWR		47	48		PWR	1.8V
3.3V	PWR		49	50		PWR	3.3V
5V	PWR		51	52		PWR	5V
12V	PWR		53	54		PWR	12V
Unused_CLKM_GPIO_0	3.3V CMOS		55	56		3.3V CMOS	Unused_CLKM_GPIO_1
Unused_CLKM_GPIO_2	3.3V CMOS		57	58		KEY_M	
	KEY_M		59	60		KEY_M	

	KEY_M KEY_M KEY_M		61 63 65	62 64 66		KEY_M KEY_M KEY_M	
Unassigned			67	68			Unassigned
Unassigned			69	70			Unassigned
Unassigned			71	72			Unassigned
Unassigned			73	74			Unassigned
Unassigned			75				

Note in the table below that the Blue and Yellow color directions are reversed compared to the data engine table. A unidirectional output from the RFM is a unidirectional input to the DE, and vice versa. Reversing the colors makes matching data busses the same color on both modules.

Pin Group	**Direction**	**Alt Function**
Power	Fixed	none
CLKIN	Differential LVDS in	Single Ended clock in
CLKOUT	Differential LVDS out	Single ended in or out
Serial Command	Fixed or I/O	none
DOUT0/DOUT1	Differential LVDS out	Single Ended in or out
DIN	Differential LVDS in	Single Ended in or out
GPIO	Fixed or I/O	none
Connector Key		

3. Mechanical Interfaces

This section describes the mechanical packaging of the clock module, including board profile, mounting and screw holes, and connector placement.

The module profile is shown in Figure 3.1. TBD. The module dimensions are TBD.

The Main electrical connector type is TBD (might be M.2?). The module mounts to the PSWS Data Engine as shown in figure 3.2 using a TBD screw at the locations shown in the profile drawing.