TangerineSDR

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Clock Module (CKM)

Requirements Document

Version Number: 0.4.1

Version Date: August 1, 2019

Document Number: TSDR-CKM-REQ

VERSION HISTORY

Version Number	Implemented By	Revision Date	Approved By	Approval Date	Description of Change
0.1, 0.2	T. McDermott	various			Original Issue, first revision.
0.3	T. McDermott	7/2/2019			Add version history. Add frequency reference for phase noise. Update Figure 1 to have only 4 synthesizer outputs. Add status message requirements. Add use cases (including other than PSWS uses). Reference the Clock Module ICD.
0.4	T. McDermott	7/18/2019			Add Variants Table and PSWS Supported note.
0.4.1	T. McDermott	August 1, 2019			Reformat and Change Document Name

1. Introduction

The Personal Space Weather Station (PSWS) Clock Module provides GPS derived time and frequency for input to the PSWS TangerineSDR receiver Data Engine (DE). It is a low cost module that provides a high accuracy pulse-per-second (PPS) timing strobe, high-accuracy UTC time, and programmable frequency synthesizer outputs derived from a GPS disciplined oscillator. The four synthesizer outputs have phase noise performance that meets the needs of the PSWS receiver. The module is intended to be programmed from the DE, and to provide timing and frequency signals to the DE. Figure 1 is a block diagram of the Clock Module.

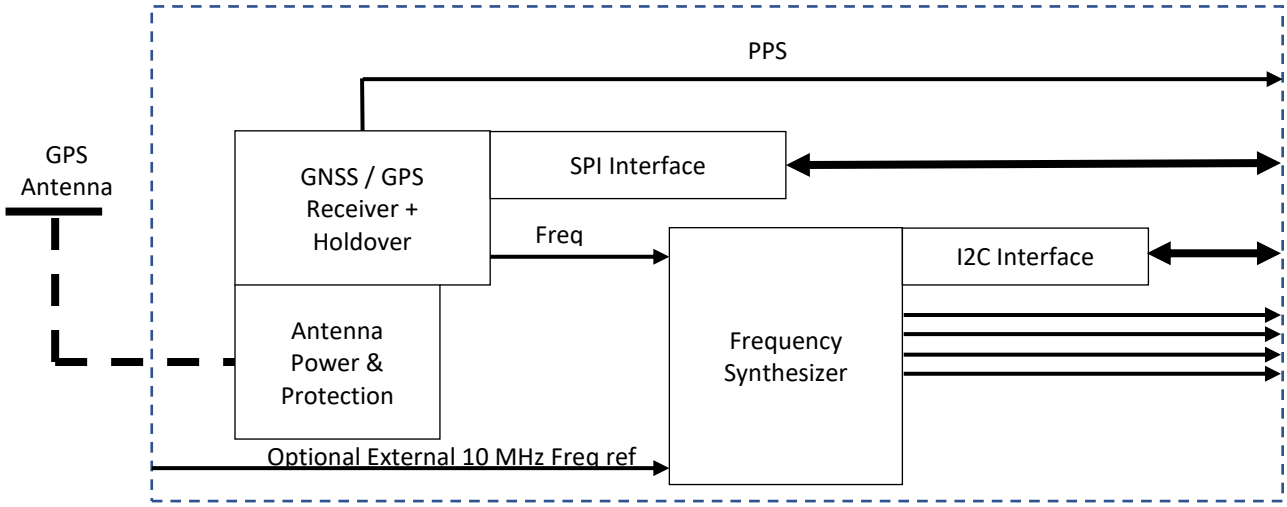

Figure 1. Block Diagram of Clock Module

The clock module contains a holdover oscillator which continues the phase and frequency outputs when GPS receiver signal is lost. It uses a low-phase-noise oscillator with frequency stability correction. The holdover oscillator may be integrated within the GPS receiver, or it may be outside the receiver but contained on the module.

1.1. Cost Goals

The cost goal of the clock module including GPS antenna is $100. It is anticipated that higher-performance (perhaps dual RF channel) GPS modules may be specified for future use, but likely at significantly higher cost. If a separate holdover oscillator / DAC / filter is needed to meet the performance requirements, the cost will likely exceed the goal by 25%.

1.2. References

The clock module form factor, mechanical layout, electrical signal interconnection, connectors and pinouts, and electrical specifications are described in a separate Interface Control Document (ICD) for the clock module.

The Local Control Channel (LCC) protocol specification describes the format of the data frames emitted by the Data Engine. Overhead within those frames will contain GPS status information as well as 64-bit NTP timing information derived from the clock module.

2. Power Supply

The Clock Module shall be powered from +3.3 VDC, and shall draw less than TBD mA (+5VDC supply is also available if needed.) The module shall provide DC-power-sourcing protected against short / open to the GPS antenna coaxial cable (the antenna including an integral low noise preamplifier) via an SMA receptacle.

3. Clock Module Outputs

The clock module provides up to 5 clock outputs that are derived from a GPS/GNSS disciplined frequency. The outputs are:

1. Synthesizer output - FPGA clock.
2. Synthesizer output - ADC clock to RF module #1.
3. Synthesizer output - ADC clock to RF module #2.
4. Synthesizer output - 10.0 MHz fixed reference output.
5. One Pulse-per-second (PPS) timing output to the FPGA.

The RF module ADC clocks shall come from synthesizer output(s) that guarantee phase stability. These ADC clock outputs must remain phase coherent across all operating conditions, DC power cycles, and restart conditions. They must utilize a stable distribution method to the DE/receiver modules.

The ADC may supply a source-synchronous data clock back to the FPGA. The clock module may also have a 10.0 MHz reference input when GPS input is not possible. Individual clock outputs shall be able to be deactivated if not used.

****Decision Needed** The electrical format (differential/voltage swing, etc.) and FPGA / ADC clock distribution method is TBD. One possibility is differential LVDS because single-ended clocks are likely to be too noisy across connectors.

The FPGA clock provides the timing to the FPGA, and may provide the ADC clock via clock distribution, or may receive the clock from the ADC via clock distribution. This decision is TBD. Typically this signal will be in the 122.88 MHz range.

The two receiver NCO signals inside the FPGA must hold a constant phase relationship. They cannot be independent oscillators that have a random phase components due to startup phase condition, or programming delay differences.

4. Clock Module Performance Requirements

The clock module shall provide various outputs meeting the following requirements.

4.1. PPS Timing Pulse Accuracy

The PPS timing pulse shall provide better than ± 50 nanosecond peak timing. This requires the use of a holdover oscillator, which may be within the GPS receiver module itself, or may be a separate oscillator, DAC, and filter on the clock module.

The timing shall meet the requirements in the absence of severe ionospheric disturbances. If there are severe disturbances then timing accuracy will be degraded to ± TBD nanoseconds.

- It is expected that a dual-channel GNSS receiver and antenna combination will be needed to maintain ± 50 nanosecond timing during severe ionospheric events. The cost and performance of that module is outside the scope of this specification and is for a later program phase.

4.1.1. Decimation and Filter Effects

Informative only: The use of decimation by the HF receiver and DE necessitates the signal be Nyquist band-limited prior to decimation. This filtering process can cause two effects:

1. The sample will be delayed by the filters used (it may require multiple different filter types, such as FIR and CIC.
2. The filter may cause non-linear phase across the receiver passband (such as a CIC filter) which will result in time variation across the receiver passband.

It is expected that the above delays will be constant from unit to unit and will be characterized during engineering analysis of the receiver. An appropriate correction table can be used by the central server if needed to normalize time difference due to

decimation. The effects are independent of the PPS, meaning that the PPS timing strobe is not impacted by them, the data samples will be altered and delayed compared to the PPS time strobe due to these effects.

4.2. Frequency Accuracy

The basic frequency accuracy of the 10.0 MHz output shall be TBD parts-per-billion (ppb) during GPS locked operation, and 100 ppb during holdover operation. The clock module frequency synthesizer shall not degrade the frequency output accuracy of its 4 outputs compared to the reference signal input significantly. The Allan Deviation (ADEV) of the clock module outputs compared against the 10.0 GPS/GNSS clock shall not deviate from the back-to-back ADEV by more than TBD.

Accuracy here is defined as compared to the GPS system defined time and frequency.

- Informative only: During measurements of the synthesizer development board, I could not find significant ADEV difference except for a few intentionally-difficult-to-synthesize frequencies.

4.3. ADC Clock

The ADC clock may need to be separately provided or may be provided via clock distribution from the FPGA. The quality of the ADC clock is critical to the performance of the entire PSWS. Excess phase noise decreases the dynamic range of the receiver and increases baseband jitter, while excess jitter degrades the noise level of the ADC at higher frequencies.

- The ADC clocks shall exhibit less than ±1 picoseconds jitter, peak.

4.4. Clock and Frequency Output Phase Noise

The various clock and synthesizer outputs are based on the frequency reference output by the GPS receiver. They should have essentially the same phase noise performance.

- The clock and synthesizer phase noise shall be less than -60 dBc at 1 Hz offset, declining as 1/f to less than -120 dBc at 1 kHz offset.
- The phase noise is specified at the NCO frequency of 30 MHz. The NCO is the internal FPGA quadrature down-conversion oscillator. (Since this point is inaccessible, the specification shall be verified by measurement of the resultant baseband signal).

4.5. Holdover Oscillator

The holdover oscillator may be internal to the GPS module or external to the GPS module, but it is contained on the clock module. It shall provide:

- Frequency stability of less than TBD ppb while GPS locked.
- Frequency stability of better than 100 ppb during the first 24 hours of holdover at a nominal temperature of 25C.
- Frequency stability of TBD ppb during the first 24 hours of holdover across a temperature range of ± TBD C.
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4.6. Status Messages

The clock module shall provide GPS status messages to the data engine via the SPI interface. The data engine may need specific electrical signal indications (rather than SPI). If so, then this section will be expanded to cover the definition of the specific electrical signals needed.

The GPS module can provide a large number of status messages to the Data Engine, the exact messages needed may change over time. Initially, the GPS module will provide the following messages for use by the data engine:

- GPS Stratum Level – the Data Engine will use this to mark overhead in the data frames using the LCC protocol. The overhead will indicate if the GPS time information is valid, degraded, or lost. The exact format of that messaged shall be described in the LCC protocol document.
- GPS failed – this will indicate a problem with the GPS module that renders it unable to acquire GPS lock.

5. Time Format

The clock module shall provide UTC time to the DE. The DE will use the UTC time and the PPS signal to time-stamp the data samples in the output frame. The intention is to time stamp data samples within ± 50 nanoseconds of GPS/GNSS time.

The DE will format the time to 64-bit NTP format time. This consists of a 32-bit Unix time seconds field, referenced against UTC time, and a 32-bit fractional second field which contains the time value of the first sample in the buffer to within ± 50 nanoseconds.

Informative only: The use of standard Unix/NTP time formats should allow the use of standard time libraries. While the Unix time format will experience numeric roll over around the year 2038, it is anticipated that the standard libraries will be modified in an

agreed, published, and well-vetted manner to accommodate this. The use of non-standard libraries can lead to a significant time keeping problems. The maintenance of a non-standard library to solve rollover problems has a strong probability of leading to additional problems.

6. Other Use Cases

The clock module may be used for applications other than the PSWS. This section describes those other use cases briefly.

The use cases are: TBD.

7. Module Variants

The Clock Module may have multiple variants optimized for different functions.

Module Variant	Physical Form	Key Use*	Key Differences
VCXO PSWS Stability.	Single M.2 connector. 2 RF SMA connectors.	PSWS.	Specified VCXO used.
Custom VCXO Stability.	Single M.2 connector, 2 RF SMA connector.	Non-PSWS.	Same physical form factor, but equipped with a non-specified oscillator.

*PSWS supported module variant: Supported by PSWS science software, firmware, hardware, programming, and data.

*Non-PSWS module variants: May be generally useful outside the PSWS project for experimentation by individuals or for other use cases, but are not planned at this time to be used to provide PSWS science data. PSWS software, firmware, and / or hardware is not planned at this time to be customized in order to provide support for non-PSWS variants, and is not planned for support by the PSWS project.