



# TangerineSDR



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*TangerineSDR*

*RF Receiver Module (RFM-5001D)*

**Interface Control Document**

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## 1. Introduction

### 1.1. Scope

There are multiple RF Modules that are planned to be defined by TAPR within the TangerineSDR program. Anticipated Modules are:

- TSDR-RXM-5000S Tangerine Receiver Module, single 12-bit 80Msps ADC
- TSDR-RXM-5000D Tangerine Receiver Module, dual 12-bit 80Msps ADC
- TSDR-RXM-5001D Tangerine Receiver Module, dual 14-bit ADC 122.88Msps
- TSDR-TXM-6000 Tangerine Transmitter Module, dual 14-bit DAC 210Msps
- TSDR-TRXM-7000 Tangerine Transceiver 70MHz - 6GHz
- TSDR-TRXM-7001 Tangerine Transceiver 10MHz - 10GHz

This document applies only to the RXM-5001D Receiver Module.

### 1.2. Module Summary: *RXM-5001D (2-channel receiver)*

This module uses two 14-bit AD converters, and is intended to support the Personal Space Weather Station (PSWS). It contains requirements in support of PSWS that may or may not exist for other receiver module variants.

The Tangerine SDR Receiver Module RXM-5001D is a dual-channel module that contains two complete receivers, from the antenna connector through the ADC. It receives two radio frequency signals in the 100 kHz to 30 MHz range, optionally filters and attenuates the signals, digitizes the signals with a low-jitter clock, and transfers the digitized samples to the Tangerine SDR Data Engine module.

The unit provides an integrated noise source that can programmatically connect each receiver to a broadband noise source of known amplitude in order to calibrate the receiver sensitivity. The unit may use a single noise source for the two receiver channels, but it will require two relays (one per channel) to select the noise source. It will also contain two plug in RF filters, two programmable attenuators, etc. The noise signal is injected ahead of the attenuator and filter. This provides the ability to capture test data that will allow determination of filter and other characteristics being applied to the received RF signal.

### 1.3. References

The main configurable component on the receiver is a dual-14-bit ADC device (one ADC per receiver channel). While the exact device has not yet been chosen, the LTC2145 14-bit ADC device is representative of one that is likely similar to the one that

will be used. The LTC6400-20 is a differential ADC driver with a fixed gain of 20 dB gain.

- LTC2145 Datasheet: <https://www.analog.com/media/en/technical-documentation/data-sheets/21454314fa.pdf>
- LVDS Specification: EIA-644. TI (National Semi) App note 971: <http://www.ti.com/lit/an/snla165/snla165.pdf>
- LTC6400-20 Datasheet: <https://www.analog.com/media/en/technical-documentation/data-sheets/640020f.pdf>

## 2. Electrical Interfaces

This section defines the electrical interfaces of the RF Module, including the connectors, connector pin outs, signals, and signal formats. Control signals are contained on a single MEC connector. External Antenna signals are on SMA connectors. The module is intended to plug onto a TangerineSDR Data Engine and interface to it via the MEC connector.

<b>J1 – Channel 1 Receive Antenna</b>				
<b>Connector type: SMA Receptacle</b>				
<b>Connector Pin #</b>	<b>Signal Name</b>	<b>Signal Electrical Format</b>	<b>Input / Output / Bidirectional</b>	<b>Description</b>
1	Receive Antenna	50 ohm RF Coaxial	I	Input – receives the 0.1 – 30 MHz signal from the channel 1 antenna.

<b>J2 – Channel 2 Receive Antenna</b>				
<b>Connector type: SMA Receptacle</b>				
<b>Connector Pin #</b>	<b>Signal Name</b>	<b>Signal Electrical Format</b>	<b>Input / Output / Bidirectional</b>	<b>Description</b>
1	Receive Antenna	50 ohm RF Coaxial	I	Input – receives the 0.1 – 30 MHz signal from the channel 2 antenna.

<b>J3 – Channel 1 Receive Filter</b>				
<b>Connector type: pair of 3 x 0.1 Inch plug-on pin receptacle strips to hold plug-on RF filter module</b>				
<b>Connector Pin #</b>	<b>Signal Name</b>	<b>Signal Electrical Format</b>	<b>Input / Output</b>	<b>Description</b>
1	GND			
2	Receive Signal	50 ohm	I	Input – receives the low level analog 0.1 – 30 MHz signal from the channel 1 antenna.
3	GND			
4	GND			
5	Filtered Signal	50 ohm	O	Output – produces the low level analog 0.1 – 30 MHz filtered signal.
6	GND			

<b>J4 – Channel 2 Receive Filter</b>				
<b>Connector type: pair of 3 x 0.1 Inch plug-on pin receptacle strips to hold plug-on RF filter module</b>				
<b>Connector Pin #</b>	<b>Signal Name</b>	<b>Signal Electrical Format</b>	<b>Input / Output</b>	<b>Description</b>
1	GND			
2	Receive Signal	50 ohm	I	Input – receives the low level analog 0.1 – 30 MHz signal from the channel 2 antenna.
3	GND			
4	GND			
5	Filtered Signal	50 ohm	O	Output – produces the low level analog 0.1 – 30 MHz filtered signal.
6	GND			

J5 – Gold edge fingers that mate to a MEC5-RA-140 RFM connector

Note the Pins numbers are WRONG and arbitrary at this time.

NAME	LVL	DIR	Pin #	Pin #	DIR	LVL	Name
GND	PWR		1	2	I	3.3V CMOS	IDENT_I2C_CLK
OSC_CLK_IN+	LVDS	I	3	4	I/O	3.3V CMOS	IDENT_I2C_DAT
OSC_CLK_IN-	LVDS	I	5	6	I/O	3.3V CMOS	SPI_MOSI / I2C_DAT
GND	PWR		7	8	O	3.3V CMOS	SPI_MISO
FPGA_CLK_IN+	LVDS	I	9	10	I	3.3V CMOS	SPI_CLK / I2C_CLK
FPGA_CLK_IN-	LVDS	I	11	12	I	3.3V CMOS	I2C_CS0n / SPI_CS0n
3.3V	PWR		13	14	I	3.3V CMOS	I2C_CS1n / SPI_CS1n
I2C_CS2n / SPI_CS2n	3.3V CMOS	I	15	16		PWR	3.3V
RFM_DOUT0_0+	LVDS	O	17	18	O	LVDS	RFM_DOUT1_0+
RFM_DOUT0_0-	LVDS	O	19	20	O	LVDS	RFM_DOUT1_0-
RFM_DOUT0_1+	LVDS	O	21	22	O	LVDS	RFM_DOUT1_1+
RFM_DOUT0_1-	LVDS	O	23	24	O	LVDS	RFM_DOUT1_1-
GND	PWR		25	26		PWR	GND
RFM_DOUT0_2+	LVDS	O	27	28	O	LVDS	RFM_DOUT1_2+
RFM_DOUT0_2-	LVDS	O	29	30	O	LVDS	RFM_DOUT1_2-
RFM_DOUT0_3+	LVDS	O	31	32	O	LVDS	RFM_DOUT1_3+
RFM_DOUT0_3-	LVDS	O	33	34	O	LVDS	RFM_DOUT1_3-
GND	PWR		35	36		PWR	GND
RFM_DOUT0_4+	LVDS	O	37	38	O	LVDS	RFM_DOUT1_4+
RFM_DOUT0_4-	LVDS	O	39	40	O	LVDS	RFM_DOUT1_4-
RFM_DOUT0_5+	LVDS	O	41	42	O	LVDS	RFM_DOUT1_5+
RFM_DOUT0_5-	LVDS	O	43	44	O	LVDS	RFM_DOUT1_5-
GND	PWR		45	46		PWR	GND
RFM_DOUT0_6+	LVDS	O	47	48	O	LVDS	RFM_DOUT1_6+
RFM_DOUT0_6-	LVDS	O	49	50	O	LVDS	RFM_DOUT1_6-
RFM_DOUT0_7+	LVDS	O	51	52	O	LVDS	RFM_DOUT1_7+
RFM_DOUT0_7-	LVDS	O	53	54	O	LVDS	RFM_DOUT1_7-
GND	PWR		55	56		PWR	GND
RFM_DOUT0_8+	LVDS	O	57	58	O	LVDS	RFM_DOUT1_8+
RFM_DOUT0_8-	LVDS	O	59	60	O	LVDS	RFM_DOUT1_8-
RFM_DOUT0_9+	LVDS	O	61	62	O	LVDS	RFM_DOUT1_9+
RFM_DOUT0_9-	LVDS	O	63	64	O	LVDS	RFM_DOUT1_9-
GND	PWR		65	66		PWR	GND
RFM_DOUT0_10+	LVDS	O	67	68	O	LVDS	RFM_DOUT1_10+
RFM_DOUT0_10-	LVDS	O	69	70	O	LVDS	RFM_DOUT1_10-
RFM_DOUT0_11+	LVDS	O	71	72	O	LVDS	RFM_DOUT1_11+
RFM_DOUT0_11-	LVDS	O	73	74	O	LVDS	RFM_DOUT1_11-
GND	PWR		75	76		PWR	GND
RFM_DOUT0_12+	LVDS	O	77	78	O	LVDS	RFM_DOUT1_12+
RFM_DOUT0_12-	LVDS	O	79	80	O	LVDS	RFM_DOUT1_12-
RFM_DOUT0_13+	LVDS	O	81	82	O	LVDS	RFM_DOUT1_13+
RFM_DOUT0_13-	LVDS	O	83	84	O	LVDS	RFM_DOUT1_13-

GND	PWR		85	86		PWR	GND
Unused RFM_DOUT0_14+	LVDS	O	87	88	O	LVDS	Unused RFM_DOUT1_14+
Unused RFM_DOUT0_14-	LVDS	O	89	90	O	LVDS	Unused RFM_DOUT1_14-
Unused RFM_DOUT0_15+	LVDS	O	91	92	O	LVDS	Unused RFM_DOUT1_15+
Unused RFM_DOUT0_15-	LVDS	O	93	94	O	LVDS	Unused RFM_DOUT1_15-
RFM_CH0_OVF+	LVDS	O	95	96	O	LVDS	RFM_CH1_OVF+
RFM_CH0_OVF-	LVDS	O	97	98	O	LVDS	RFM_CH1_OVF-
GND	PWR		99	100		PWR	GND
Unused RFM_DIN_0+	LVDS	I	101	102	I	LVDS	Unused RFM_DIN_2+
Unused RFM_DIN_0-	LVDS	I	103	104	I	LVDS	Unused RFM_DIN_2-
Unused RFM_DIN_1+	LVDS	I	105	106	I	LVDS	Unused RFM_DIN_3+
Unused RFM_DIN_1-	LVDS	I	107	108	I	LVDS	Unused RFM_DIN_3-
GND	PWR		109	110		PWR	GND
Unused RFM_DIN_4+	LVDS	I	111	112	I	LVDS	Unused RFM_DIN_6+
Unused RFM_DIN_4-	LVDS	I	113	114	I	LVDS	Unused RFM_DIN_6-
Unused RFM_DIN_5+	LVDS	I	115	116	I	LVDS	Unused RFM_DIN_7+
Unused RFM_DIN_5-	LVDS	I	117	118	I	LVDS	Unused RFM_DIN_7-
GND	PWR		119	120		PWR	GND
Unused RFM_DIN_8+	LVDS	I	121	122	I	LVDS	Unused RFM_DIN_11+
Unused RFM_DIN_8-	LVDS	I	123	124	I	LVDS	Unused RFM_DIN_11-
Unused RFM_DIN_9+	LVDS	I	125	126	I	LVDS	Unused RFM_DIN_12+
Unused RFM_DIN_9-	LVDS	I	127	128	I	LVDS	Unused RFM_DIN_12-
Unused RFM_DIN_10+	LVDS	I	129	130	I	LVDS	Unused RFM_DIN_13+
Unused RFM_DIN_10-	LVDS	I	131	132	I	LVDS	Unused RFM_DIN_13-
1.8V	PWR		133	134		PWR	1.8V
CLKOUT0+	LVDS	O	135	136	O	LVDS	CLKOUT+
CLKOUT0-	LVDS	O	137	138	O	LVDS	CLKOUT1-
5.0V	PWR		139	140		PWR	+12V

Note in the table below that the Blue and Yellow color directions are reversed compared to the data engine table. A unidirectional output from the RFM is a unidirectional input to the DE, and vice versa. Reversing the colors makes matching data busses the same color on both modules.

Pin Group	Direction	Alt Function
Power	Fixed	none
CLKIN	Differential LVDS in	Single Ended clock in
CLKOUT	Differential LVDS out	Single ended in or out
Serial Command	Fixed or I/O	none
DOUT0/DOUT1	Differential LVDS out	Single Ended in or out
DIN	Differential LVDS in	Single Ended in or out



## 2.1. I2C and SPI Device Addressing

All RF modules implement an Identification EPROM that allows the FPGA on the Data Engine to configure the I/O signals to match the module type plugged in (within FPGA capability limits). The Identification EPROM is connected separately from other I2C devices.

Device	I2C Address	Chip Select
<b>I2C Identification EPROM</b>	-	CS not used (EPROM always selected)

The RXM-5100D implements three other I2C devices. The I2C addresses of these devices are listed in the table. The Chip Select state needed to select the device is listed. The I2C devices share Clock lines, Data lines, and Chip Selects with the SPI Interface due to connector pin limitations.

Device	I2C Address	Chip Select
<b>Chan 0 Attenuator</b>	TBD	CS0n=0 CS1n=0 CS2n=0
<b>Chan 1 Attenuator</b>	TBD	CS0n=0 CS1n=1 CS2n=0
<b>General Purpose I/O</b>	Address 0 Bit 0 controls the Noise Relays. 0 = Noise Deselected. 1 = Noise Selected. Other Addresses and Bits Unused.	CS0n=1 CS1n=0 CS2n=0

The RXM-5100D implements one SPI device.

Device	SPI Address	Chip Select
<b>ADC Configuration Registers</b>	TBD	CS2n=1

### **3. Mechanical Interfaces**

This section describes the mechanical packaging of the clock module, including board profile, mounting and screw holes, and connector placement.

The module profile is shown in Figure 3.1. TBD. The module dimensions are TBD.

The Main electrical connector type is SamTec MEC 140 pin, 0.5mm spacing. The module mounts to the PSWS Data Engine as shown in figure 3.2 using a TBD screw at the locations shown in the profile drawing.