TangerineSDR

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RF Receiver Module (RFM-5001D)

Interface Control Document

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VERSION HISTORY

Version Number	Implemented By	Revision Date	Approved By	Approval Date	Description of Change
0.1	T. McDermott	August 8, 2019			Original Issue
0.2	T. McDermott	November 21, 2019			Change 140-pin connector pin definitions, and plug-on-filter pin connectors (4-pin vs. 3-pin connector). Change the ADC and ADC driver chips and datasheet references. Update I2C and SPI tables.
0.2.1	T. McDermott	November 22, 2019			Change J5 pin 13 from Ground to +3.3V
0.3	T. McDermott	March 7, 2020			Update connector pinout to match actual routed board prototype. Schematic revision XA9. Add jumpers and resistor select descriptions.

1. Introduction

1.1. Scope

There are multiple RF Modules that are planned to be defined by TAPR within the TangerineSDR program. Anticipated Modules are:

- TSDR-RXM-5000S Tangerine Receiver Module, single 12-bit 80Msps ADC
- TSDR-RXM-5000D Tangerine Receiver Module, dual 12-bit 80Msps ADC
- TSDR-RXM-5001D Tangerine Receiver Module, dual 14-bit ADC 122.88Msps
- TSDR-TXM-6000 Tangerine Transmitter Module, dual 14-bit DAC 210Msps
- TSDR-TRXM-7000 Tangerine Transceiver 70MHz - 6GHz
- TSDR-TRXM-7001 Tangerine Transceiver 10MHz - 10GHz

This document applies only to the RXM-5001D Receiver Module.

1.2. Module Summary: RXM-5001D (2-channel receiver)

This module uses two 14-bit AD converters, and is intended to support the Personal Space Weather Station (PSWS). It contains requirements in support of PSWS that may or may not exist for other receiver module variants.

The Tangerine SDR Receiver Module RXM-5001D is a dual-channel module that contains two complete receivers, from the antenna connector through the ADC. It receives two radio frequency signals in the 100 kHz to 30 MHz range, optionally filters and attenuates the signals, digitizes the signals with a low-jitter clock, and transfers the digitized samples to the Tangerine SDR Data Engine module.

The unit provides an integrated noise source that can programmatically connect each receiver to a broadband noise source of known amplitude in order to calibrate the receiver sensitivity. The unit uses a single noise source for the two receiver channels, but it will require two relays (one per channel) to select the noise source. It will also contain two plug in RF filters, two programmable attenuators, etc. The noise signal is injected ahead of the attenuator and filter. This provides the ability to capture test data that will allow determination of filter and other characteristics being applied to the received RF signal.

1.3. References

The main configurable component on the receiver is a dual-14-bit ADC device (one ADC per receiver channel), the Analog Devices AD9648. The LTC6420-20 is a dual-channel differential ADC driver with a fixed gain of 20 dB gain.

- AD9648 Datasheet: https://www.analog.com/media/en/technical-documentation/data-sheets/AD9648.pdf
- LVDS Specification: EIA-644. TI (National Semi) App note 971: http://www.ti.com/lit/an/snla165/snla165.pdf
- LTC6420-20 Datasheet: https://www.analog.com/media/en/technical-documentation/data-sheets/642020fb.pdf

2. Electrical Interfaces

This section defines the electrical interfaces, jumpers, and resistor-selectable signals of the RF Module, including the connectors, connector pin outs, signals, and signal formats. Control signals are contained on a single MEC connector. External Antenna signals are on SMA connectors. The module is intended to plug onto a TangerineSDR Date Engine and interface to it via the MEC connector.

2.1. RF Connectors

J2 – Channel 1 Receive Antenna Connector type: SMA Receptacle				
Connector Pin #	**Signal Name**	**Signal Electrical Format**	**Input / Output / Bidirectional**	**Description**
1	Receive Antenna	50 ohm RF Coaxial	I	Input – receives the 0.1 – 30 MHz signal from the channel 1 antenna.

J7 – Channel 2 Receive Antenna Connector type: SMA Receptacle				
Connector Pin #	**Signal Name**	**Signal Electrical Format**	**Input / Output / Bidirectional**	**Description**
1	Receive Antenna	50 ohm RF Coaxial	I	Input – receives the 0.1 – 30 MHz signal from the channel 2 antenna.

J4 – Channel 1 Receive Filter Input Connector type: 4 x 0.1 Inch plug-on pin receptacle strip to hold plug-on RF filter module				
Connector Pin #	**Signal Name**	**Signal Electrical Format**	**Input / Output**	**Description**
1	GND			
2	Receive Signal	50 ohm	I	Input – receives the low level analog 0.1 – 30 MHz signal from the channel 1 antenna.
3	Receive Signal			Wired in parallel with pin 2
4	GND			

J5 – Channel 1 Receive Filter Output Connector type: 4 x 0.1 Inch plug-on pin receptacle strip to hold plug-on RF filter module				
Connector Pin #	**Signal Name**	**Signal Electrical Format**	**Input / Output**	**Description**
1	GND			
2	Filtered Signal	50 ohm	O	Output – produces the low level analog 0.1 – 30 MHz filtered signal.
3	Filtered Signal	50 ohm	O	Wired in parallel with pin 2
4	GND			

J10 – Channel 2 Receive Filter Input Connector type: 4 x 0.1 Inch plug-on pin receptacle strip to hold plug-on RF filter module				
Connector Pin #	**Signal Name**	**Signal Electrical Format**	**Input / Output**	**Description**
1	GND			
2	Receive Signal	50 ohm	I	Input – receives the low level analog 0.1 – 30 MHz signal from the channel 1 antenna.
3	Receive Signal	50 ohm	I	Wired in parallel with pin 2
4	GND			

J11 – Channel 2 Receive Filter Output Connector type: 4 x 0.1 Inch plug-on pin receptacle strip to hold plug-on RF filter module				
Connector Pin #	**Signal Name**	**Signal Electrical Format**	**Input / Output**	**Description**
1	GND			
2	Filtered Signal	50 ohm	O	Output – produces the low level analog 0.1 – 30 MHz filtered signal.
3	Filtered Signal	50 ohm	O	Wired in parallel with pin 2
4	GND			

J6 – Channel 1 Receive Filter Power Option Connector type: 10 x 0.1 Inch plug-on pin receptacle strip to hold plug-on Active RF filter module type (not used for passive RF filter module).				
Connector Pin #	**Signal Name**	**Signal Electrical Format**	**Input / Output**	**Description**
1	Analog Gnd 1			Channel 1 RF Ground
2	+5 VDC		I	+5 VDC supply voltage to active filter module
3	Analog Gnd 1			Channel 1 RF Ground
4	Digital Gnd			Common for power supply returns.
5	Analog Gnd 1			Channel 1 RF Ground
6	Digital Gnd			Common for power supply returns.
7	Analog Gnd 1			Channel 1 RF Ground
8	+3.3 VDC		I	+3.3 VDC supply voltage to active filter module
9	NC			
10	NC			

J8 – Channel 2 Receive Filter Power Option Connector type: 10 x 0.1 Inch plug-on pin receptacle strip to hold plug-on Active RF filter module type (not used for passive RF filter module).				
Connector Pin #	**Signal Name**	**Signal Electrical Format**	**Input / Output**	**Description**
1	Analog Gnd 2			Channel 2 RF Ground
2	+5 VDC		I	+5 VDC supply voltage to active filter module
3	Analog Gnd 2			Channel 2 RF Ground
4	Digital Gnd			Common for power supply returns.
5	Analog Gnd 2			Channel 2 RF Ground
6	Digital Gnd			Common for power supply returns.
7	Analog Gnd 2			Channel 2 RF Ground
8	+3.3 VDC		I	+3.3 VDC supply voltage to active filter module
9	NC			
10	NC			

2.2. Jumpers

Jumpers are used to select certain options. Some of the jumpers are paralleled with a zero-ohm resistor, which is normally not installed on the board (DNI – Do Not Install). Make sure the zero-ohm resistor is not installed if you wish to open the jumper setting

JP1 – Channel 1 Receive Filter Bypass **Connector type: 2 x 0.1 Inch plug-on pin receptacle.**
If Channel 1 does not have a receive filter installed, then insert the jumper to provide signal continuity around the missing filter.

JP2 – Channel 2 Receive Filter Bypass **Connector type: 2 x 0.1 Inch plug-on pin receptacle.**
If Channel 2 does not have a receive filter installed, then insert the jumper to provide signal continuity around the missing filter.

JP3 – Power to noise generator **Connector type: 2 x 0.1 Inch plug-on pin receptacle.**
If JP3 is not installed then all power is removed from the noise generator circuitry. Computer control of the noise generator is disabled. **Install JP3 if you wish to be able to use the noise generator, and to turn it on and off under Computer control.**

JP4 – Channel 1 Receive Ground Bonding **Connector type: 2 x 0.1 Inch plug-on pin receptacle.**
Install this jumper to bond the RF common connection of Channel 1 to the system ground if desired or if needed for other reasons.

JP5 – Channel 2 Receive Ground Bonding **Connector type: 2 x 0.1 Inch plug-on pin receptacle.**
Install this jumper to bond the RF common connection of Channel 2 to the system ground if desired or if needed for other reasons.

2.3. Resistor Select (ADC Clock Source)

The ADC clock normally is sourced from the high-performance GPS disciplined clock source. This is enabled by leaving the normally installed zero ohm resistors R45 and R46 intact. If you wish to instead source the ADC clock from the (much lower performance FPGA source) then remove R45 and R46 and instead install zero ohm resistors at R47 and R48 respectively.

2.4. Digital and Power Connector

Note that J1 connector pin data busses, over-range, and clock out functionality changes dependent on whether the ADC is programmed in CMOS or LVDS DDR mode.
The schematic for the module defines both of these cases (read the notes). Which mode is utilized will be decided after testing. LVDS DDR mode requires 245.76 Mbits/sec operation on the data bus pins which may be too fast for the FPGA. However LVDS should reduce the digital noise level.

J1 – MEC5-RA-140 RFM connector
Note that the pins are ADC-chip mode dependent. The definition in the table below is DDR LVDS mode. If the mode needs to be changed to CMOS, then the table will need to be updated.

NAME	LVL	DIR	Pin #	Pin #	DIR	LVL	Name
GND	PWR		1	2	I	3.3V CMOS	IDENT_I2C_CLK
OSC_CLK_IN+	LVDS	I	3	4	I/O	3.3V CMOS	IDENT_I2C_DAT
OSC_CLK_IN-	LVDS	I	5	6	I/O	3.3V CMOS	CTRL_I2C_DAT
GND	PWR		7	8			
FPGA_CLK_IN+	LVDS	I	9	10	I	3.3V CMOS	CTRL_I2C_CLK
FPGA_CLK_IN-	LVDS	I	11	12			
3.3V	PWR		13	14			
			15	16		PWR	3.3V
			17	18			
SYNC	1.8V CMOS	I	19	20			
DUMMY+ (not used in LVDS mode)	LVDS	O	21	22			
DUMMY- (not used in LVDS mode)	LVDS	O	23	24			
GND	PWR		25	26		PWR	GND
RFM_DOUT0-	LVDS	O	27	28			
RFM_DOUT0+	LVDS	O	29	30			
RFM_DOUT1-	LVDS	O	31	32			
RFM_DOUT1-	LVDS	O	33	34			
GND	PWR		35	36		PWR	GND
RFM_DOUT2-	LVDS	O	37	38			
RFM_DOUT2+	LVDS	O	39	40			
RFM_DOUT3-	LVDS	O	41	42			
RFM_DOUT3-	LVDS	O	43	44			
GND	PWR		45	46		PWR	GND
RFM_DOUT4-	LVDS	O	47	48			
RFM_DOUT4+	LVDS	O	49	50			
RFM_DOUT5-	LVDS	O	51	52			
RFM_DOUT5-	LVDS	O	53	54			
GND	PWR		55	56		PWR	GND
RFM_DOUT6-	LVDS	O	57	58			
RFM_DOUT6+	LVDS	O	59	60			

RFM_DOUT7-	LVDS	O	61	62			
RFM_DOUT7-	LVDS	O	63	64			
GND	PWR		65	66		PWR	GND
RFM_DOUT8-	LVDS	O	67	68			
RFM_DOUT8+	LVDS	O	69	70			
RFM_DOUT9-	LVDS	O	71	72			
RFM_DOUT9-	LVDS	O	73	74			
GND	PWR		75	76		PWR	GND
RFM_DOUT10-	LVDS	O	77	78			
RFM_DOUT10+	LVDS	O	79	80			
RFM_DOUT11-	LVDS	O	81	82			
RFM_DOUT11-	LVDS	O	83	84			
GND	PWR		85	86		PWR	GND
RFM_DOUT12-	LVDS	O	87	88			
RFM_DOUT12+	LVDS	O	89	90			
RFM_DOUT13-	LVDS	O	91	92			
RFM_DOUT13-	LVDS	O	93	94			
RFM_CH0_OVF-	LVDS	O	95	96			
RFM_CH0_OVF+	LVDS	O	97	98			
GND	PWR		99	100		PWR	GND
SPI_BIDIR_1.8V	1.8V CMOS	I/O	101	102			
SPI_SCLK_1.8V	1.8V CMOS	I	103	104			
SPI_CSELn_1.8V	1.8V CMOS	I	105	106			
			107	108			
GND	PWR		109	110		PWR	GND
			111	112			
			113	114			
			115	116			
			117	118			
GND	PWR		119	120		PWR	GND
			121	122			
			123	124			
			125	126			
			127	128			
			129	130			
			131	132			
+1.8V	PWR		133	134		PWR	+5V
DAT_CLK_OUT0-	LVDS	O	135				
DAT_CLK_OUT0+	LVDS	O	137				
+5V	PWR		139	140		PWR	+12V

Note in the table below that the Blue and Yellow color directions are reversed compared to the data engine table. A unidirectional output from the RFM is a unidirectional input to the DE, and vice versa. Reversing the colors makes matching data busses the same color on both modules.

Pin Group	Direction	Alt Function
Power	Fixed	none
CLKIN	Differential LVDS in	Single Ended clock in
CLKOUT	Differential LVDS out	Single ended in or out
Serial Command	Fixed or I/O	none
DOUT0/DOUT1	Differential LVDS out	Single Ended in or out
DIN	Differential LVDS in	Single Ended in or out
Serial Command 1.8V or CMOS control 1.8V	Input, Output, and I/O	

2.5. I2C and SPI Device Addressing

All RF modules implement an Identification EPROM that allows the FPGA on the Data Engine to configure the I/O signals to match the module type plugged in (within FPGA capability limits). The Identification EPROM is connected separately from other I2C devices.

Device	I2C Address	Chip Select
I2C Identification EPROM	-	CS not used (EPROM always selected)

The RXM-5100D implements a control interface consisting of an octal latch to drive the relays and one status LED. These occur of different I2C pins than the EPROM I2C.

Device	I2C Address	Chip Select
Control Output Register	000	CS not used (Control latch always selected)
Bit 0	Low = Channel 1 Noise Relay Enable	
Bit 1	Low = Channel 1 10 dB attenuator enable	
Bit 2	Low = Channel 1 20 dB attenuator enable	
Bit 3	Low = Channel 2 Noise Relay Enable	
Bit 4	Low = Channel 2 10 dB attenuator enable	
Bit 5	Low = Channel 2 20 dB attenuator enable	
Bit 6	Low = Turn on Green status LED	
Bit 7	Low = Turn on Red status LED	

The AD9648 ADC uses a 3-wire SPI interface. The data line is bidirectional rather than the traditional MISO and MOSI lines used in SPI.

Device	SPI Address	Chip Select
AD9648 Dual-channel ADC	-	CSEL = 0 to enable. CSEL needs to be

		toggled to update some modes.

3. Mechanical Interfaces

This section describes the mechanical packaging of the clock module, including board profile, mounting and screw holes, and connector placement.

The module profile is shown in Figure 3.1. TBD. The module dimensions are TBD.

The Main electrical connector type is SamTec MEC 140 pin, 0.5mm spacing. The module mounts to the PSWS Data Engine as shown in figure 3.2 using two #4-40 screws at the locations shown in the profile drawing.