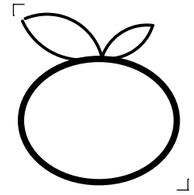
Rev	Date	Name	Description
XA1	29Oct2020	WA2DFI	Initial Drawing
XA2	14Feb2021	WA2DFI	Update Clocks, I/O, complete first draft - release to CAD
XA3	23Feb2021	WA2DFI	Clean up comment pages, add VCCIO to LEAF
XA4	25Feb2021	WA2DFI	Fix decal names
XA5	25Feb2021	WA2DFI	Continued cleanup
XA6	03Mar2021	WA2DFI	Add VCCIO for LEAF, fix power connector
XA7	15Mar2021	WA2DFI	Move CLK9 termination resistor
XA8	30Mar2021	WA2DFI	Add holes. Swap D3 pins. Swap T1 pins.
XA9	16Apr2021	WA2DFI	Update U26 decal name
XA10	27Apr2021	WA2DFI	First round of pin swap: USB2
XA11	4May2021	WA2DFI	Second round of pin swap: USB3
XA12	5May2021	WA2DFI	Third round of pin swap
XA13	6May2021	WA2DFI	Update U6 and U14 PCB shapes. More pin swaps
XA14	6May2021	WA2DFI	More pin swaps
XA15	7May2021	WA2DFI	More pin swaps
XA16	11May2021	WA2DFI	More pin swaps
XA17	12May2021	WA2DFI	Change U7 to KSZ9896C
XA18	20May2021	WA2DFI	Change KSZ9896C VCCIO to 3.3V
XA19	21May2021	WA2DFI	Change Bank 1A power to VCCIO27
XA20	28May2021	WA2DFI	Pin Swaps
XA21	4Jun2021	WA2DFI	Add resistors to LVDS, add SS DESC, split DDR3 VTT
XA22	7Jun2021	WA2DFI	Fix net names
XA23	11Jun2021	WA2DFI	Adjust Power Supply caps
XA24	1Jul2021	WA2DFI	Swap out caps C153 & C155 for 1.0mm thick types
XA25	9Jul2021	WA2DFI	Add USB connector to CKM port
XA26	13Jul2021	WA2DFI	Cover Page changes



Design By Scotty Cowling WA2DFI

Zephyr Engineering Inc.

Title: TangerineSDR Data Engine

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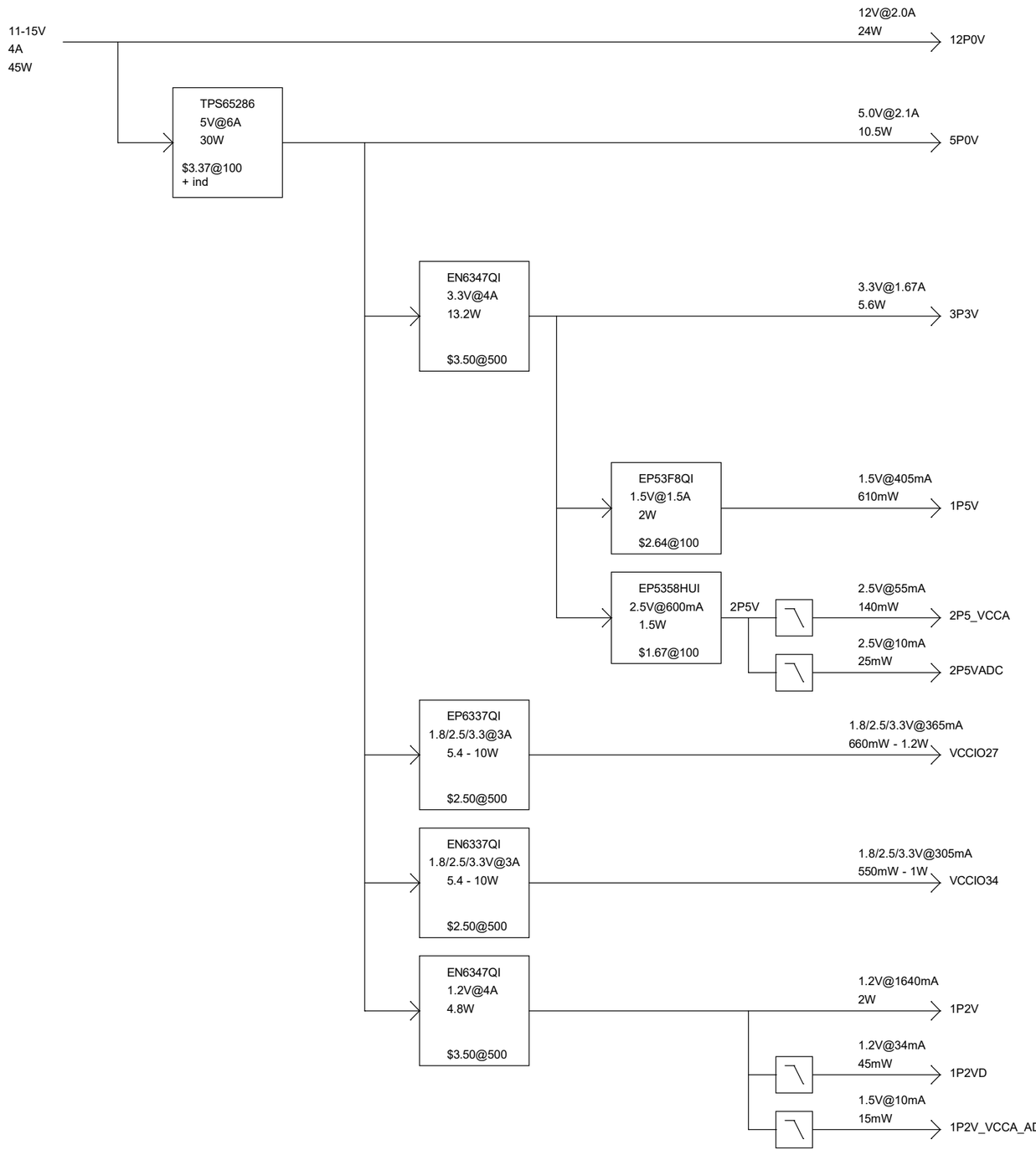

RFM0 (500mA)
RFM1 (500mA)
CKM (500mA)
LEAF (500mA)

USB 2.0 (500mA)
RFM0/1 (500mA)
CKM (500mA)
LEAF (500mA)
FAN (100mA)
uSDHC (100mA)

FPGA VCCIO1 (100mA)
FPGA VCCIO8 (70mA)
GbE PHY & I/O (175mA)
USB 2.0 (35mA)
USB 3.0 (195mA)
QSPI (40mA)
uSDHC (500mA)
TEMP, EEPROM (25mA)
RFM0/1 (200mA)
LEAF (100mA)
BUZZER/LED (320mA)
CKM (500mA)

DDR3 (275mA)
FPGA VCCIO6 (125mA)
FPGA OSC (3mA)
uSDHC (10mA)
CKM (50mA)

MAX10 PLL (55mA)

MAX10 ADC (10mA)

RFM0 (65mA)
FPGA VDDIO2 (125mA)
FPGA VDDIO7 (125mA)
CKM (50mA)

RFM1 (65mA)
FPGA VDDIO3 (90mA)
FPGA VDDIO4 (150mA)
CKM (50mA)

MAX10 CORE (1200mA)
GbE CORE (440mA)

MAX10 PLL (34mA)

MAX10 ADC (10mA)

PS NET NAMES

1P2V	FPGA VCC/GbE CORE
1P2V_VCCD_PLL	FPGA VCCD_PLL
1P5V_DDR3	DDR3
2P5V_VCCA	FPGA VCCA
2P5_VCCA_ADC	FPGA VCCA_ADC
1P2V_VCCINT	FPGA VCCINT
VCCIO27	FPGA VCCIO2/VCCIO7
VCCIO34	FPGA VCCIO3/VCCIO4
3P3V	RFM0/1, CKM
5P0V	RFM0/1, CKM
12P0V	RFM0/1, CKM

REGULATOR OUTPUTS

12P0V	POWER INPUT (11-15V@4A)
5P0V	TPS65286 (5V@6A)
3P3V	EN6347QI (3.3V@4A)
1P2V	EN6347QI (1.2V@4A)
VCCIO27	EN6337QI (1.8V/2.5V/3.3V@3A)
VCCIO34	EN6337QI (1.8V/2.5V/3.3V@3A)
2P5V	EP5358HUI (2.5V@600mA)
1P5V	EP53F8QI (1.5V@1.5A)

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Title: TangerineSDR DE PS Block

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PLL USAGE

ETH	DDR3
CLK0 CLK1	CLK2 CLK3
CLK4 CLK5	CLK4 CLK5
PLL3/PLL_T	PLL2/PLL_R
PLL1/PLL_L	PLL4/PLL_B
CLK0 CLK1	CLK2 CLK3
CLK6 CLK7	CLK6 CLK7
RFM0	RFM1

OPTION: SYNTHDO CKM

SI5344B/D

PD

OSC 10-30M

FPGA

SYN 0 — VCCIO_0 (VCCIO27) 2 — CKM_LEAF_CLK 2 — LEAF

SYN 1 — VCCIO_1 (VCCIO34) 2

SYN 2 — VCCIO_2 (1.8V) 2

SYN 3 — VCCIO_3 (3.3V) 2

EXT_REF_IN 2

REF_CLK_OUT 1

EFC_OUT 1

N/C

PPS_IN

10M_IN

DAC

GPS

RESET_INn 1

CKM_10M 1

SYNC_OUTn 1

EFC_IN 1

PLL_LOCK 1

I2C0_COMM 2

I2C1_COMM 2

GPS_PPS 1

GPSDO_PPS 1

OPTION: BASIC CKM

SI53343 x2

LPF

OSC 122.88M

VCCIO_0 (VCCIO27)

VCCIO_1 (VCCIO34)

VCCIO_2 (1.8V)

VCCIO_3 (3.3V)

EXT_REF_IN 2

REF_CLK_OUT 1

EFC_OUT 1

N/C

10M REF

SCHMITT TRIG

RESET_INn 1

CLK_10M 1

SYNC_OUTn 1

EFC_IN 1

PLL_LOCK 1

I2C0_COMM 2

I2C1_COMM 2

GPS_PPS 1

GPSDO_PPS 1

N/C

RFM0

CKM_RFM0_CLK 2 — OSC IN — CLK OUT — 2 RFM0_FPGA_CLK0

VCCIO27

FPGA_RFM0_CLK 2 — FPGA IN — CLK OUT — 2 RFM0_FPGA_CLK1

RFM1

CKM_RFM1_CLK 2 — OSC IN — CLK OUT — 2 RFM1_FPGA_CLK0

VCCIO34

FPGA_RFM1_CLK 2 — FPGA IN — CLK OUT — 2 RFM1_FPGA_CLK1

3P3V — OSC 50MHz

OSC 25MHz — 3P3V

1P5V — LVL TRANS

VCCIO27

VCCIO34

VCCIO34

VCCIO27

PLL_L

PLL_B

BANK2 BANK4

RFM CLOCKS OUT

DDR3 OSC_50M

CLK2p

BANK6

(1.5V)

OSC_MAX10

CLK5n

BANK8

(3.3V)

CLK7 CLK6 CLK1 CLK0

BANK3 BANK2

RFM CLOCKS IN

CKM_FPGA_CLK 2

LEAF_FPGA_CLK 1

CKM_FPGA_10M 1

CKM_FPGA_SYNCn 1

CLK3 BANK6 (1.5V)

CLK4p BANK8 (3.3V)

CLK4n BANK8 (3.3V)

DPCLK1 BANK2 (VCCIO27) (OD)

FPGA_CKM_EFC 1

CKM_FPGA_PLL_LOCK 1

FPGA_CKM_I2C0_COMM 2

FPGA_CKM_I2C1_COMM 2

CKM_FPGA_GPS_PPS 1

CKM_FPGA_GPSDO_PPS 1

I/O BANK1B (3.3V)

I/O BANK5 (3.3V TOL)

I/O BANK5 (1.5V OD)

I/O BANK5 (1.5V OD)

I/O BANK6 (1.5V)

I/O BANK6 (1.5V)

CKM COMMS

FPGA

(1.5V) BANK6 PLL_R — I/O

RESET MON

(OD) (1.5V) BANK6 CLK2n — RESETn (OD)

USB3

(3.3V) BANK8 CLK5p — USB3_CLK — 3.3V

(I/O only) (3.3V) BANK8 PLL_Tn — I/O

ETH0

(3.3V) BANK8 PLL_Tp — ETH0_TXCLK

(VCCIO27) BANK2 DPCLK0 — ETH0_RXCLK — 3.3V

DDR3

DPCLK2/DQSN2R — DDR3_DQS0_n

DPCLK3/DQS2R — DDRs_DQS0_p

DQSN3R — DDR3_DQS1_n

DQS3R — DDR3_DQS1_p

CK#_6 — DDR3_CK_n

CK_6 — DDR3_CK_p

BANK6 (1.5V) — 1.5V

Zephyr Engineering Inc.

Title: TangerineSDR DE Clock Distribution

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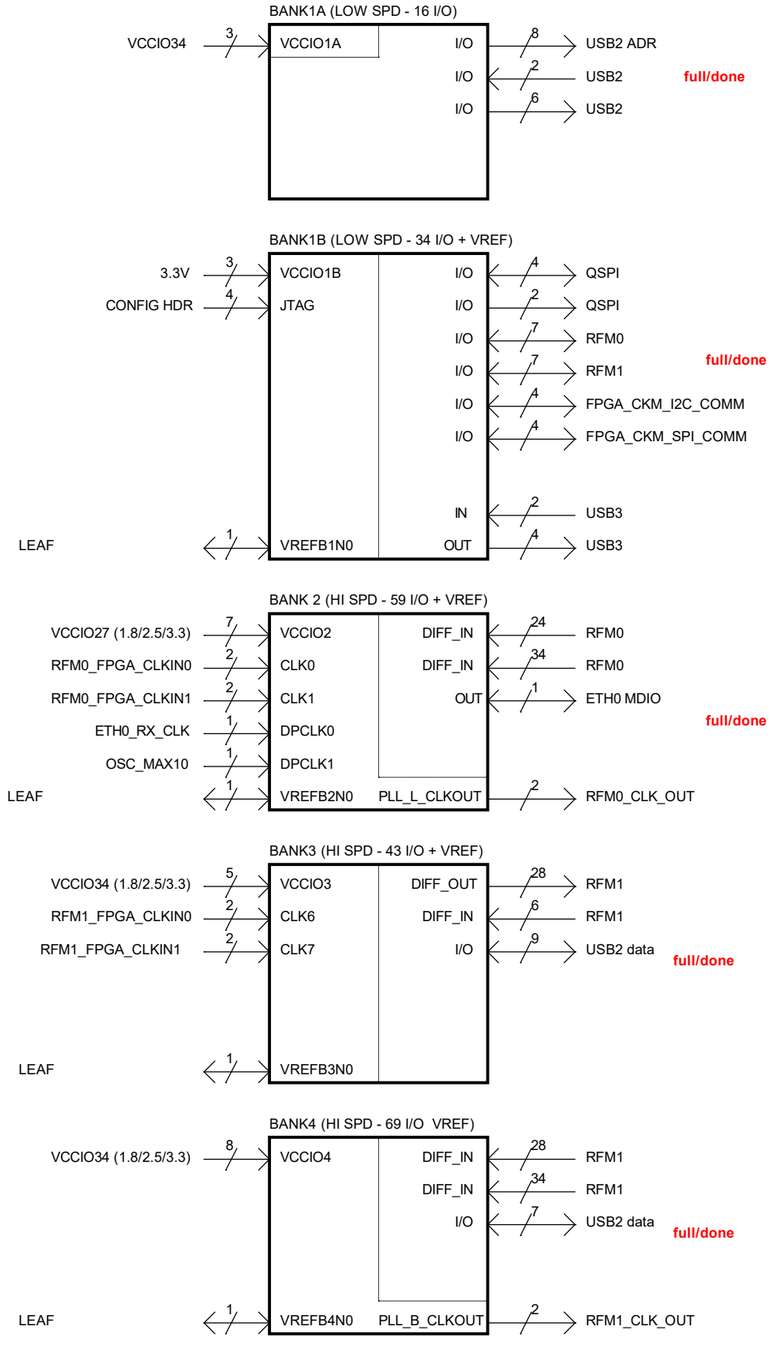
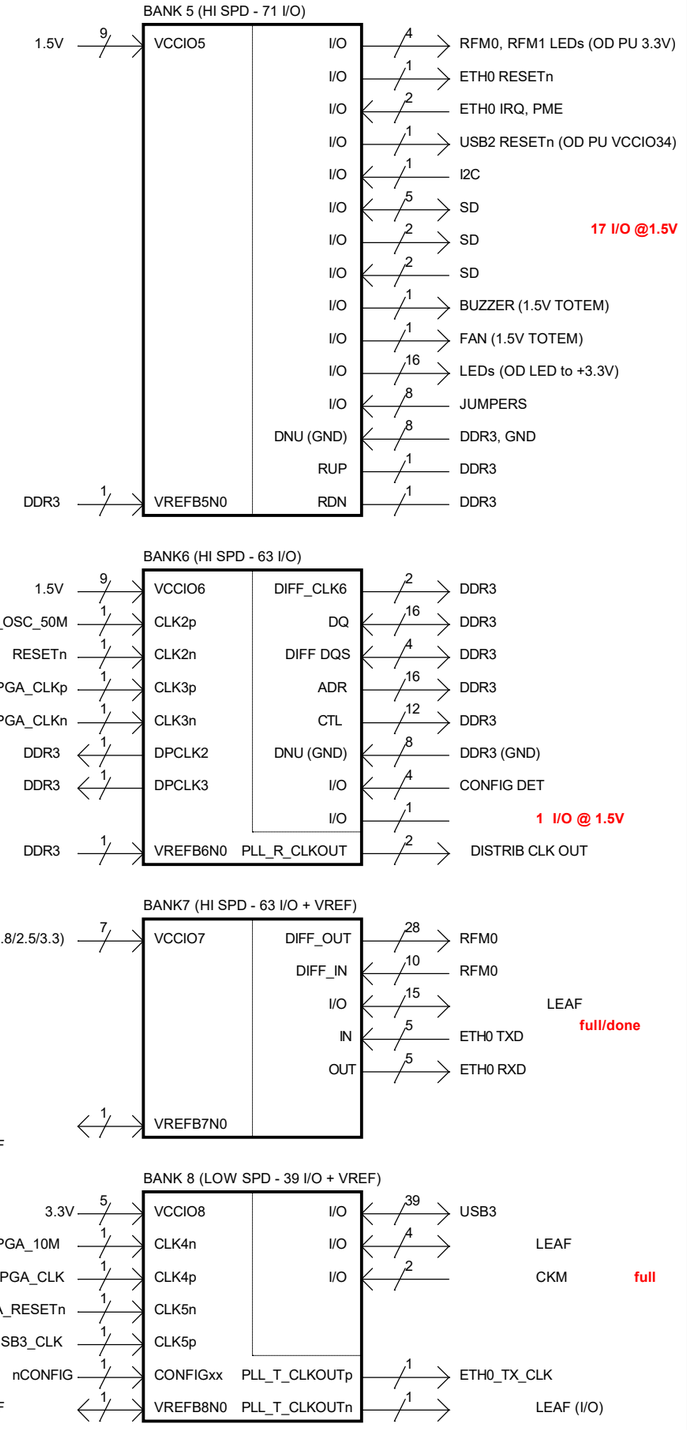


	LOGIC BLOCK	I/O VOLTS	BANK	QTY	
	RFM0	VCCIO27	2	58 diff in	
	RFM0	VCCIO27	7	10 diff in	
	RFM0	VCCIO27	7	28 diff out	
	RFM0	VCCIO27	2	4 diff ck in	112
	RFM0	VCCIO27	2	2 diff ck out	
	RFM0	3.3V	1B	7 se i/o	
	RFM0	1.5V/3.3V	5	2 LED open drain	
	RFM1	VCCIO34	3	6 diff in	
	RFM1	VCCIO34	3	28 diff out	
	RFM1	VCCIO34	4	62 diff in	
	RFM1	VCCIO34	3	4 diff ck in	112
	RFM1	VCCIO34	4	2 diff ck out	
	RFM1	3.3V	1B	7 se i/o	
	RFM1	1.5V/3.3V	5	2 LED open drain	
	DDR3	1.5V	6	22 assigned	
	DDR3	1.5V	6	27 unassigned	
	DDR3	1.5V	5	0 unassigned	51
	DDR3	1.5V	6	2 clk out	
	ETH0	VCCIO27	2	1 i/o	275
	ETH0	VCCIO27	7	5 TXD out	
	ETH0	VCCIO27	7	5 RXD in	
	ETH0	1.5V	5	1 RESETn OD out	
	ETH0	3.3V	8	1 MDC out	
	ETH0	1.5V	5	1 OD IRQ in	17
	ETH0	1.5V	5	1 OD PME in	
	ETH0	3.3V	8	1 TX_CLK out	
	ETH0	VCCIO27	2	1 RX_CLK in	
	USB2	VCCIO34	1A	8 adr out	
	USB2	VCCIO34	3	9 data i/o	
	USB2	VCCIO34	4	7 data i/o	33
	USB2	VCCIO34	1A	2 in	
	USB2	VCCIO34	5	1 RESETn out	
	USB2	VCCIO34	1A	6 out	
	USB3	3.3V	8	32 data i/o	325
	USB3	3.3V	8	4 byte enab i/o	
	USB3	3.3V	8	3 ctl i/o	46
	USB3	3.3V	1B	2 in	
	USB3	3.3V	1B	4 out	
	USB3	3.3V	8	1 clk in	
P8,9	LOCAL_I2C	3.3V	5	1 OD i/o, 1 OD out	
P19	LOCAL_I2C	3.3V	8	1 out	6
	LOCAL_I2C	1.5V	5	3 in	
P5	QSPI	3.3V	1B	4 i/o	377
P19	QSPI	3.3V	1B	2 out	6
P8	uSDHC	1.5V	5	5 SE i/o	
P20	uSDHC	1.5V	5	2 OD out/2 out	11
	uSDHC	1.5V	5	2 in	
P8,9	BUZZER	VCCO27	2	1 out	
P21	FAN	1.5V	5	1 out	18
	LEDs	1.5V	5	16 OD out	
	Jumpers	1.5V	5	8 in	
	OSC_30.72M	3.3V	8	1 clk in	
	OSC_50M	1.5V	6	1 clk in	420
	CKM	3.3V		4 in	
	CKM	3.3V		2 out	16
	CKM	3.3V		1 i/o	
	CKM	3.3V	8	1 clk in	
	CKM	3.3V	1B	4 comm (dual I2C)	
	CKM	3.3V	1B	4 comm (SPI)	
	RPi EXP	3.3V	8	4 i/o	
	RPi EXP	3.3V	1B	1 slow i/o	6
	RPi EXP	3.3V	8	1 slow i/o	
	RESETn	1.5V	6	1 OD in	442
	LEAF EXP	3.3V	1B	7 slow i/o	
	LEAF EXP	VCCIO27	7	15 i/o	21
	LEAF EXP	VCCIO27	2, 7	2 slow i/o	
	LEAF EXP	VCCIO34	3, 4	2 slow i/o	
	Config Det	1.5V	5, 6	4 in	8
	JTAG HDR	3.3V	1B	4 i/o	
	TOTAL			471	

s/b 37 unused I/O?



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Title: MAX10 DE Bank Assignments

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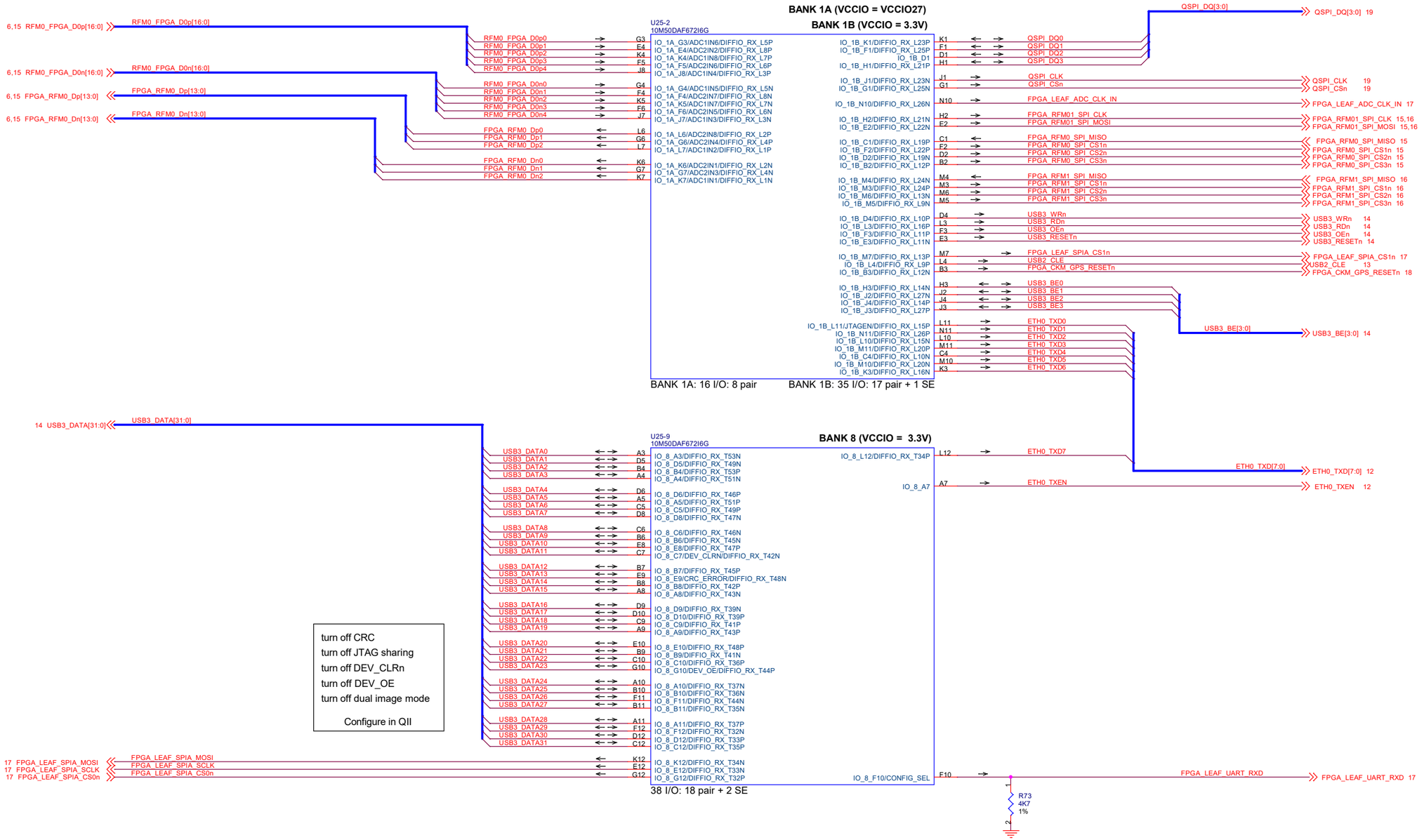

Zephyr Engineering Inc.	Title: TangerineSDR DE FPGA Banks 1A, 1B and 8	
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5,15 RFM0_FPGA_D0p[16:0]
5,15 RFM0_FPGA_D0n[16:0]
15 RFM0_FPGA_D1p[16:0]
15 RFM0_FPGA_D1n[16:0]

U25-3
10M50DAF672I6G

BANK 2 (VCCIO27 = 1.8V/2.5V/3.3V)

RFM0_FPGA_D0p5	W3	IO_2_W3/DIFFIO_RX_L48P	
RFM0_FPGA_D0p6	V2	IO_2_V2/DIFFIO_RX_L42P	
RFM0_FPGA_D0p7	U5	IO_2_U5/DIFFIO_RX_L46P	
RFM0_FPGA_D0p8	T10	IO_2_T10/DIFFIO_RX_L41P	
RFM0_FPGA_D0n5	V4	IO_2_V4/DIFFIO_RX_L48N	
RFM0_FPGA_D0n6	U1	IO_2_U1/DIFFIO_RX_L42N	
RFM0_FPGA_D0n7	U6	IO_2_U6/DIFFIO_RX_L46N	
RFM0_FPGA_D0n8	U10	IO_2_U10/DIFFIO_RX_L41N	
RFM0_FPGA_D0p9	R7	IO_2_R7/DIFFIO_RX_L34P	
RFM0_FPGA_D0p10	P4	IO_2_P4/DIFFIO_RX_L31P	
RFM0_FPGA_D0p11	N4	IO_2_N4/DIFFIO_RX_L39P	
RFM0_FPGA_D0p12	V3	IO_2_V3/DIFFIO_RX_L43P	
RFM0_FPGA_D0n9	R6	IO_2_R6/DIFFIO_RX_L34N	
RFM0_FPGA_D0n10	R4	IO_2_R4/DIFFIO_RX_L31N	
RFM0_FPGA_D0n11	N5	IO_2_N5/DIFFIO_RX_L39N	
RFM0_FPGA_D0n12	U2	IO_2_U2/DIFFIO_RX_L43N	
RFM0_FPGA_D0p13	T3	IO_2_T3/DIFFIO_RX_L37P	
RFM0_FPGA_D0p14	P1	IO_2_P1/DIFFIO_RX_L33P	
RFM0_FPGA_D0p15	M1	IO_2_M1/DIFFIO_RX_L29P	
RFM0_FPGA_D0p16	N3	IO_2_N3/DIFFIO_RX_L32P	
RFM0_FPGA_D0n13	R2	IO_2_R2/DIFFIO_RX_L37N	
RFM0_FPGA_D0n14	P2	IO_2_P2/DIFFIO_RX_L33N	
RFM0_FPGA_D0n15	N1	IO_2_N1/DIFFIO_RX_L29N	
RFM0_FPGA_D0n16	M2	IO_2_M2/DIFFIO_RX_L32N	
RFM0_FPGA_D1p0	AA5	IO_2_AA5/DIFFIO_RX_L51P	
RFM0_FPGA_D1p1	AD2	IO_2_AD2/DIFFIO_RX_L55P	
RFM0_FPGA_D1p2	W6	IO_2_W6/DIFFIO_RX_L53P	
RFM0_FPGA_D1p3	AC1	IO_2_AC1/DIFFIO_RX_L56P	
RFM0_FPGA_D1n0	AA4	IO_2_AA4/DIFFIO_RX_L51N	
RFM0_FPGA_D1n1	AD1	IO_2_AD1/DIFFIO_RX_L55N	
RFM0_FPGA_D1n2	W7	IO_2_W7/DIFFIO_RX_L53N	
RFM0_FPGA_D1n3	AB1	IO_2_AB1/DIFFIO_RX_L56N	
RFM0_FPGA_D1p4	AB3	IO_2_AB3/DIFFIO_RX_L60P	
RFM0_FPGA_D1p5	W5	IO_2_W5/DIFFIO_RX_L57P	
RFM0_FPGA_D1p6	W1	IO_2_W1/DIFFIO_RX_L44P	
RFM0_FPGA_D1p7	V6	IO_2_V6/DIFFIO_RX_L47P	
RFM0_FPGA_D1n4	AC2	IO_2_AC2/DIFFIO_RX_L60N	
RFM0_FPGA_D1n5	Y5	IO_2_Y5/DIFFIO_RX_L57N	
RFM0_FPGA_D1n6	V1	IO_2_V1/DIFFIO_RX_L44N	
RFM0_FPGA_D1n7	V7	IO_2_V7/DIFFIO_RX_L47N	
RFM0_FPGA_D1p8	U4	IO_2_U4/DIFFIO_RX_L40P	
RFM0_FPGA_D1p9	T4	IO_2_T4/DIFFIO_RX_L45P	
RFM0_FPGA_D1p10	P3	IO_2_P3/DIFFIO_RX_L35P	
RFM0_FPGA_D1n8	U3	IO_2_U3/DIFFIO_RX_L40N	
RFM0_FPGA_D1n9	T5	IO_2_T5/DIFFIO_RX_L45N	
RFM0_FPGA_D1n10	R3	IO_2_R3/DIFFIO_RX_L35N	
RFM0_FPGA_D1p12	AB4	IO_2_AB4/DIFFIO_RX_L58P	
RFM0_FPGA_D1p13	AA2	IO_2_AA2/DIFFIO_RX_L49P	
RFM0_FPGA_D1p14	Y2	IO_2_Y2/DIFFIO_RX_L50P	
RFM0_FPGA_D1p15	AA3	IO_2_AA3/DIFFIO_RX_L54P	
RFM0_FPGA_D1n12	AC3	IO_2_AC3/DIFFIO_RX_L58N	
RFM0_FPGA_D1n13	AA1	IO_2_AA1/DIFFIO_RX_L49N	
RFM0_FPGA_D1n14	Y1	IO_2_Y1/DIFFIO_RX_L50N	
RFM0_FPGA_D1n15	Y3	IO_2_Y3/DIFFIO_RX_L54N	
RFM0_FPGA_D1p16	Y4	IO_2_Y4/DIFFIO_RX_L52P	
RFM0_FPGA_D1n16	W4	IO_2_W4/DIFFIO_RX_L52N	
BUZ_ON	R1	IO_2_R1	

IO_2_P10/DIFFIO_RX_L30P	P10	FPGA_RFM0_Dp8	
IO_2_P11/DIFFIO_RX_L30N	P11	FPGA_RFM0_Dn8	

59 I/O: 29 pair + 1 SE

FPGA_RFM0_Dp[13:0] → FPGA_RFM0_Dp[13:0] 5,15
FPGA_RFM0_Dn[13:0] → FPGA_RFM0_Dn[13:0] 5,15

3P3V
VCCIO27

C103 100nF 10V
C106 100nF 10V

U4
74AVC1T45GW-Q100H
VCCA VCCB
A B
DIR GND

17 FPGA_LEAF_GPS_FIX_IN → FPGA_LEAF_GPS_FIX_IN

3P3V
VCCIO27

C105 100nF 10V
C108 100nF 10V

U2
74AVC1T45GW-Q100H
VCCA VCCB
A B
DIR GND

17 FPGA_LEAF_GPS_PPS1 → FPGA_LEAF_GPS_PPS1

21 BUZ_ON → BUZ_ON

U25-8
10M50DAF672I6G

BANK 7 (VCCIO27 = 1.8V/25.V/3.3V)

RFM0_FPGA_D1p11	C13	IO_7_C13/DIFFIO_RX_T30P	
RFM0_FPGA_D1n11	B13	IO_7_B13/DIFFIO_RX_T30N	
	G17	IO_7_G17/DIFFIO_RX_T7P	
	E17	IO_7_E17/DIFFIO_RX_T9P	
	E16	IO_7_E16/DIFFIO_RX_T9N	
	K15	IO_7_K15/DIFFIO_RX_T17P	
	L15	IO_7_L15/DIFFIO_RX_T17N	
	C16	IO_7_C16/DIFFIO_RX_T19P	
	E18	IO_7_E18/DIFFIO_RX_T10P	
FPGA_LEAF_GPS_FIX_IN_F	D18	IO_7_D18/DIFFIO_RX_T10N	
FPGA_LEAF_GPS_PPS1_F	D17	IO_7_D17/DIFFIO_RX_T19N	
FPGA_LEAF_GPS_PPS2_F	F17	IO_7_F17/DIFFIO_RX_T7N	
USB2_AD0	A12	IO_7_A12/DIFFIO_RX_T31N	
USB2_AD1	B12	IO_7_B12/DIFFIO_RX_T31P	
USB2_AD2	A13	IO_7_A13/DIFFIO_RX_T20N	
USB2_AD3	C14	IO_7_C14/DIFFIO_RX_T27N	
USB2_AD4	A14	IO_7_A14/DIFFIO_RX_T29P	
USB2_AD5	A15	IO_7_A15/DIFFIO_RX_T25N	
USB2_AD6	B15	IO_7_B15/DIFFIO_RX_T23N	
USB2_AD7	C15	IO_7_C15/DIFFIO_RX_T27P	
USB2_AD8	A16	IO_7_A16/DIFFIO_RX_T25P	
USB2_AD9	B16	IO_7_B16/DIFFIO_RX_T23P	
USB2_AD10	C17	IO_7_C17/DIFFIO_RX_T13N	
USB2_AD11	A18	IO_7_A18	
USB2_AD12	B18	IO_7_B18/DIFFIO_RX_T16N	
USB2_AD13	C18	IO_7_C18/DIFFIO_RX_T13P	
USB2_AD14	A19	IO_7_A19/DIFFIO_RX_T14N	
USB2_AD15	B19	IO_7_B19/DIFFIO_RX_T16P	
USB2_ALE	D22	IO_7_D22/DIFFIO_RX_T2P	
USB2_CSn	C19	IO_7_C19/DIFFIO_RX_T12N	
USB2_DACK	C22	IO_7_C22/DIFFIO_RX_T2N	
USB2_DREQ	B22	IO_7_B22/DIFFIO_RX_T1P	
USB2_INT	E20	IO_7_E20/DIFFIO_RX_T3N	
USB2_RDn	D19	IO_7_D19/DIFFIO_RX_T12P	
USB2_WRn	F20	IO_7_F20/DIFFIO_RX_T3P	

IO_7_L14/DIFFIO_RX_T22P	L14	FPGA_RFM0_Dp3	
IO_7_E14/DIFFIO_RX_T24P	E14	FPGA_RFM0_Dp4	
IO_7_F15/DIFFIO_RX_T18P	F15	FPGA_RFM0_Dp5	
IO_7_G15/DIFFIO_RX_T15P	G15	FPGA_RFM0_Dp6	
IO_7_K14/DIFFIO_RX_T22N	K14	FPGA_RFM0_Dn3	
IO_7_D13/DIFFIO_RX_T24N	D13	FPGA_RFM0_Dn4	
IO_7_E15/DIFFIO_RX_T18N	E15	FPGA_RFM0_Dn5	
IO_7_F16/DIFFIO_RX_T15N	F16	FPGA_RFM0_Dn6	
IO_7_G13/DIFFIO_RX_T26P	G13	FPGA_RFM0_Dp7	
IO_7_D15/DIFFIO_RX_T21P	D15	FPGA_RFM0_Dp9	
IO_7_L13/DIFFIO_RX_T28P	L13	FPGA_RFM0_Dp10	
IO_7_G14/DIFFIO_RX_T20P	G14	FPGA_RFM0_Dp11	
IO_7_F13/DIFFIO_RX_T26N	F13	FPGA_RFM0_Dn7	
IO_7_D14/DIFFIO_RX_T21N	D14	FPGA_RFM0_Dn9	
IO_7_K13/DIFFIO_RX_T28N	K13	FPGA_RFM0_Dn10	
IO_7_F14/DIFFIO_RX_T20N	F14	FPGA_RFM0_Dn11	
IO_7_G18/DIFFIO_RX_T11P	G18	FPGA_RFM0_Dp12	
IO_7_G19/DIFFIO_RX_T5P	G19	FPGA_RFM0_Dp13	
IO_7_F18/DIFFIO_RX_T11N	F18	FPGA_RFM0_Dn12	
IO_7_F19/DIFFIO_RX_T5N	F19	FPGA_RFM0_Dn13	
IO_7_A20/DIFFIO_RX_T14P	A20	USB2_A0	
IO_7_C20/DIFFIO_RX_T6N	C20	USB2_A1	
IO_7_D20/DIFFIO_RX_T4P	D20	USB2_A2	
IO_7_A21/DIFFIO_RX_T8N	A21	USB2_A3	
IO_7_B21/DIFFIO_RX_T8P	B21	USB2_A4	
IO_7_C21/DIFFIO_RX_T6P	C21	USB2_A5	
IO_7_D21/DIFFIO_RX_T4N	D21	USB2_A6	
IO_7_A22/DIFFIO_RX_T1N	A22	USB2_A7	

63 I/O: 31 pair + 1 SE

USB2_A[7:0] → USB2_A[7:0] 13

14 USB3_RXFn → USB3_RXFn
14 USB3_TXEn → USB3_TXEn
17 LEAF_FPGA_ADC_CLK_OUT → LEAF_FPGA_ADC_CLK_OUT
17 LEAF_FPGA_CLK_SYNC_OUT → LEAF_FPGA_CLK_SYNC_OUT
17 LEAF_FPGA_SPIA_MISO → LEAF_FPGA_SPIA_MISO
17 LEAF_FPGA_UART_TXD → LEAF_FPGA_UART_TXD
12 ETH0_RXDV → ETH0_RXDV

3P3V
VCCIO27

C104 100nF 10V
C107 100nF 10V

U3
74AVC1T45GW-Q100H
VCCA VCCB
A B
DIR GND

17 FPGA_LEAF_GPS_PPS2 → FPGA_LEAF_GPS_PPS2

13 USB2_AD[15:0] → USB2_AD[15:0]

13 USB2_ALE → USB2_ALE
13 USB2_CSn → USB2_CSn
13 USB2_DACK → USB2_DACK
13 USB2_DREQ → USB2_DREQ
13 USB2_INT → USB2_INT
13 USB2_RDn → USB2_RDn
13 USB2_WRn → USB2_WRn

Zephyr Engineering Inc.

Title: TangerineSDR DE FPGA Banks 2, 7

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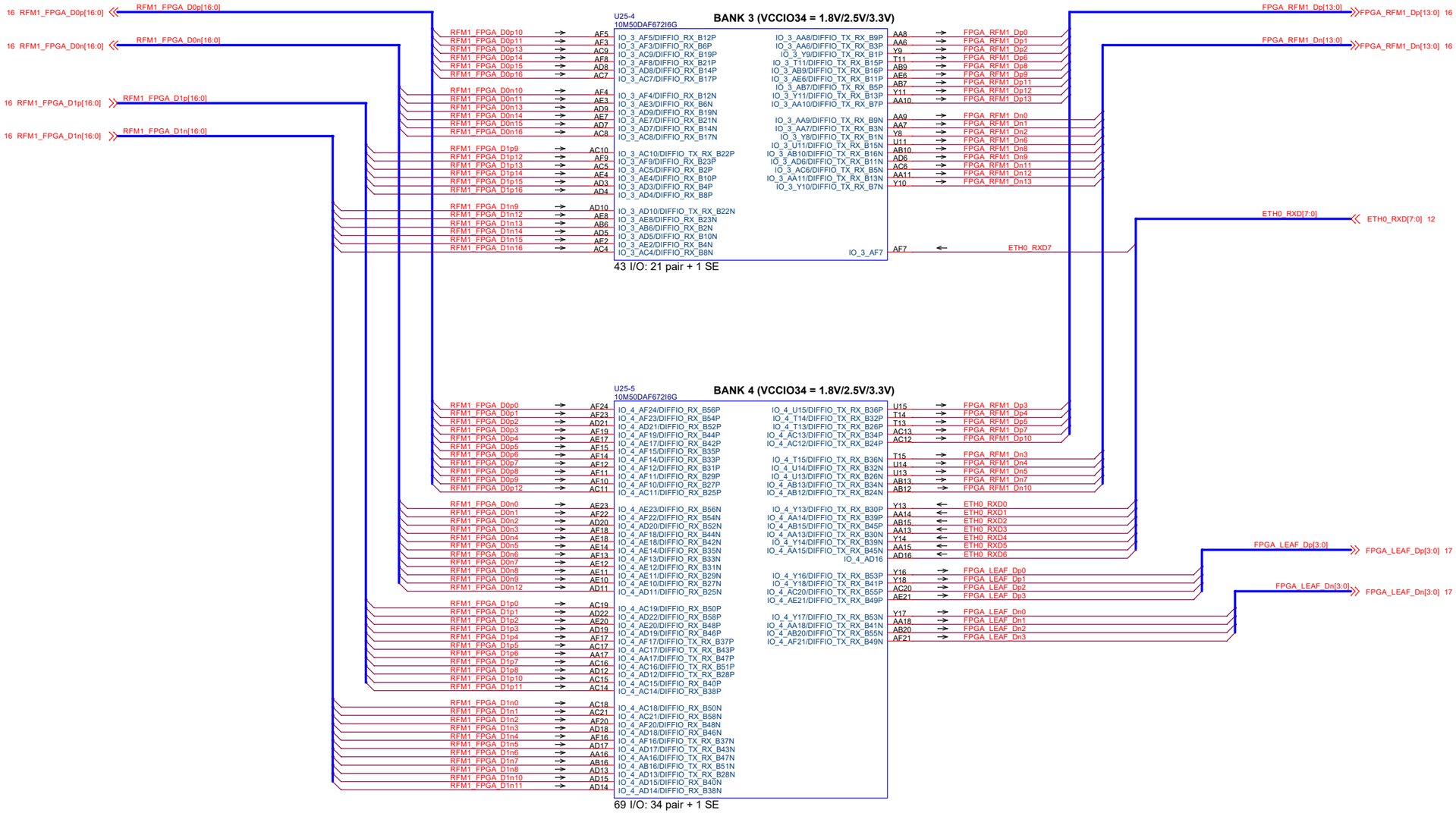

Zephyr Engineering Inc.

Title: TangerineSDR DE FPGA Banks 3 and 4

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OD to 1.5V
OD to 1.5V
OD to 3.3V

OD LED to 3.3V

O.D. VCCIO34 PU

FIXED PINS

U25-6
10M50DAF672I6G

BANK 5 (VCCIO = 1.5V)

71 I/O: 35 pair + 1 SE

OD LED to 3.3V

U25-7
10M50DAF672I6G

BANK 6 (VCCIO = 1.5V)

63 I/O: 31 pair + 1 SE

FIXED PINS

SWAP OK amongst DDR3_DQ[7:0] plus pin L23

SWAP OK amongst DDR3_DQ[15:8] plus pin H22

FIXED PINS

Zephyr Engineering Inc.	Title: TangerineSDR DE FPGA Banks 5 and 6	
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FROM RFM0

FROM RFM1

TO GLOBAL RST

FROM CKM

FROM USB3

FROM LEAF

FROM CKM

15 RFM0_FPGA_CLK0n
15 RFM0_FPGA_CLK0p
15 RFM0_FPGA_CLK1n
15 RFM0_FPGA_CLK1p

16 RFM1_FPGA_CLK0n
16 RFM1_FPGA_CLK0p
16 RFM1_FPGA_CLK1n
16 RFM1_FPGA_CLK1p

12,18 RESETn
18 CKM_FPGA_CLKn
18 CKM_FPGA_CLKp

14 USB3_CLK
17 LEAF_FPGA_CLK
18 CKM_FPGA_GPS_CLK

U25-10
10M50DAF672I6G

MAX10 CLOCK

BANK 2 VCCIO27=1.8V/2.5V/3.3V

IO_2_P7/CLK0N/DIFFIO_RX_L28N — P7
IO_2_P6/CLK0P/DIFFIO_RX_L28P — P6
IO_2_R11/CLK1N/DIFFIO_RX_L36N — R11
IO_2_R10/CLK1P/DIFFIO_RX_L36P — R10
IO_2_T6/DPCLK0/DIFFIO_RX_L38N — T6 — ETH0_RXCLK — ETH0_RXCLK 12
IO_2_R5/DPCLK1/DIFFIO_RX_L38P — R5 — CKM_FPGA_SYNCn — CKM_FPGA_SYNCn 18
IO_2_Y6/PLL_L_CLKOUTP/DIFFIO_RX_L59P — Y6 — FPGA_RFM0_CKp — FPGA_RFM0_CLKp 15
IO_2_Y7/PLL_L_CLKOUTN/DIFFIO_RX_L59N — Y7 — FPGA_RFM0_CKn — FPGA_RFM0_CLKn 15

BANK 3 VCCIO34=1.8V/2.5V/3.3V

IO_3_U12/CLK7N/DIFFIO_TX_RX_B20N — U12
IO_3_T12/CLK7P/DIFFIO_TX_RX_B20P — T12
IO_3_AA12/CLK6N/DIFFIO_TX_RX_B18N — AA12
IO_3_Y12/CLK6P/DIFFIO_TX_RX_B18P — Y12

BANK 4 VCCIO34=1.8V/2.5V/3.3V

IO_4_AB19/PLL_B_CLKOUTP/DIFFIO_TX_RX_B57P — AB19 — FPGA_RFM1_CLKp — FPGA_RFM1_CLKp 16
IO_4_AB18/PLL_B_CLKOUTN/DIFFIO_TX_RX_B57N — AB18 — FPGA_RFM1_CLKn — FPGA_RFM1_CLKn 16

BANK 6 VCCIO6=1.5V

IO_6_N25/CLK2N/DIFFIO_RX_R38N — N25
IO_6_N24/CLK2P/DIFFIO_RX_R38P — N24
IO_6_M24/CLK3N/DIFFIO_RX_R40N — M24
IO_6_M25/CLK3P/DIFFIO_RX_R40P — M25
IO_6_E21/PLL_R_CLKOUTN/DIFFIO_RX_R69N — F21 — CKM_FPGA_GPS_PPS — CKM_FPGA_GPS_PPS 17,18
IO_6_E22/PLL_R_CLKOUTP/DIFFIO_RX_R69P — E22 — ETH0_CLK125 — ETH0_CLK125 12

BANK 8 VCCIO8=3.3V

IO_8_D11/CLK4N/DIFFIO_RX_T38N — D11
IO_8_E11/CLK4P/DIFFIO_RX_T38P — E11
IO_8_K10/CLK5N/DIFFIO_RX_T40N — K10
IO_8_K11/CLK5P/DIFFIO_RX_T40P — K11
IO_8_D7/PLL_T_CLKOUTN/DIFFIO_RX_T52N — D7 — LEAF_FPGA_RESETn — LEAF_FPGA_RESETn 17
IO_8_E7/PLL_T_CLKOUTP/DIFFIO_RX_T52P — E7 — ETH0_TXCLK — ETH0_TXCLK 12

26 I/O

FROM ETH0
FROM CKM (OD)
TO RFM0
TO RFM0
TO RFM1
FROM CKM
FROM ETH0
FROM LEAF
TO ETH0

3P3V
R137 4K7 1%
R140 120R 1%
R143 169R 1%
R139 120R 1%
R119 4K7 1%
U31 STM1818R (VCC, RSTn, VSS)
S1 SW_PB_MOM_SPST
RESET
C73 100nF 10V
1P5V
C65 100nF 10V
C69 100nF 10V
U21 74AVC1T45GW-Q100H (VCCA, VCCB, A, B, DIR, GND)
U20 S333025T-50.000-X-CT (VDD, EN, OUT, GND)
OSC_50M_33
OSC_50M15
R54 33R 1%
C175 100nF 10V
OSC_50M15R
U27 S333025T-25.000-X-CT
OSC_25M
R62 33R 1%
OSC_25MR
C322 100nF 10V

U25-11
10M50DAF672I6G

BANK 1B (VCCIO = 3.3V)
BANK 8 (VCCIO = 3.3V)

IO_1B_N7/TDI/DIFFIO_RX_L18N — FPGA_TDI — N7
IO_1B_C2/TMS/DIFFIO_RX_L17N — FPGA_TMS — C2
IO_1B_N6/TDO/DIFFIO_RX_L18P — FPGA_TDO — N6
IO_1B_D3/TCK/DIFFIO_RX_L17P — FPGA_TCK — D3
IO_8_F8/CONF_DONE/DIFFIO_RX_T50N — F8 — CONF_DONE — PU during conf
IO_8_F9/NSTATUS/DIFFIO_RX_T50P — F9 — nSTATUS — PU during conf
INPUT_ONLY_8_G9/NCONFIG — G9 — nCONFIG — PU during conf

0 I/O

DONE
Green DS12
R112 10K 1%
R113 150R 1%
R128 10K 1%
Q1 IRLML6244TRPbF
R130 10K 1%
R129 10K 1%
R131 1K 1%
R127 10K 1%
D7 BAT54CV,115
PROGRAM
J11 HDR_2x5_0.100_vert
C274 100nF 10V
C313 10pF 50V
C314 10pF 50V
C315 10pF 50V
C316 10pF 50V

U25-12
10M50DAF672I6G

G5 ANAIN1__G5
J5 ANAIN2__J5
J6 ADC_VREF__J6
IO_1B_E1/VREFB1N0 — E1 — FPGA_LEAF_MAG_EN — FPGA_LEAF_MAG_EN 17 — 3.3V Output
IO_8_A6/VREFB8N0 — A6 — LOCAL_I2C_WEn — LOCAL_I2C_WEn 19
IO_3_AF6/VREFB3N0 — AF6 — ETH0_MDC — ETH0_MDC 12 — O.D. VCCIO34 Output
IO_4_AE15/VREFB4N0 — AE15 — ETH0_MDIO — ETH0_MDIO 12 — O.D. VCCIO34 I/O
IO_7_A17/VREFB7N0 — A17 — CKM_FPGA_AUX_CLK0 — CKM_FPGA_AUX_CLK0 18
IO_2_T1/VREFB2N0 — T1 — CKM_FPGA_AUX_CLK1 — CKM_FPGA_AUX_CLK1 18 — VCCIO27 - 3.3V Input
IO_5_V26/VREFB5N0 — V26
IO_6_G25/VREFB6N0 — G25
DNU__L2 — L2

8 I/O

1P5V
R57 1K 1%
C72 100nF DNI 10V
FPGA_VREF
R58 1K 1%
C196 100nF 10V
C194 100nF 10V
Place next to FPGA pins
Group together & next to FPGA

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Title: TangerineSDR DE FPGA Clocks, JTAG

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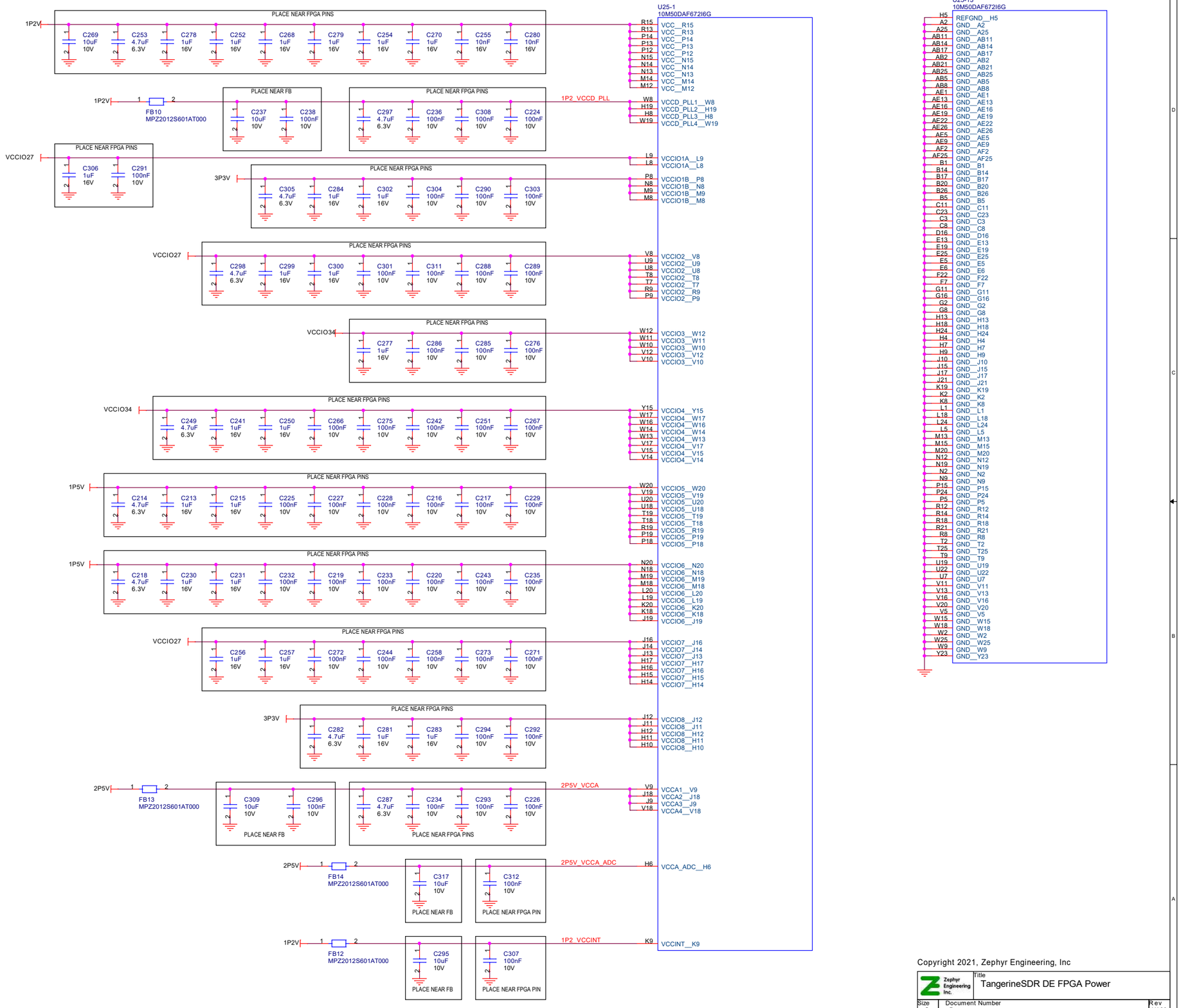

Zephyr Engineering Inc.	Title: TangerineSDR DE FPGA Power	
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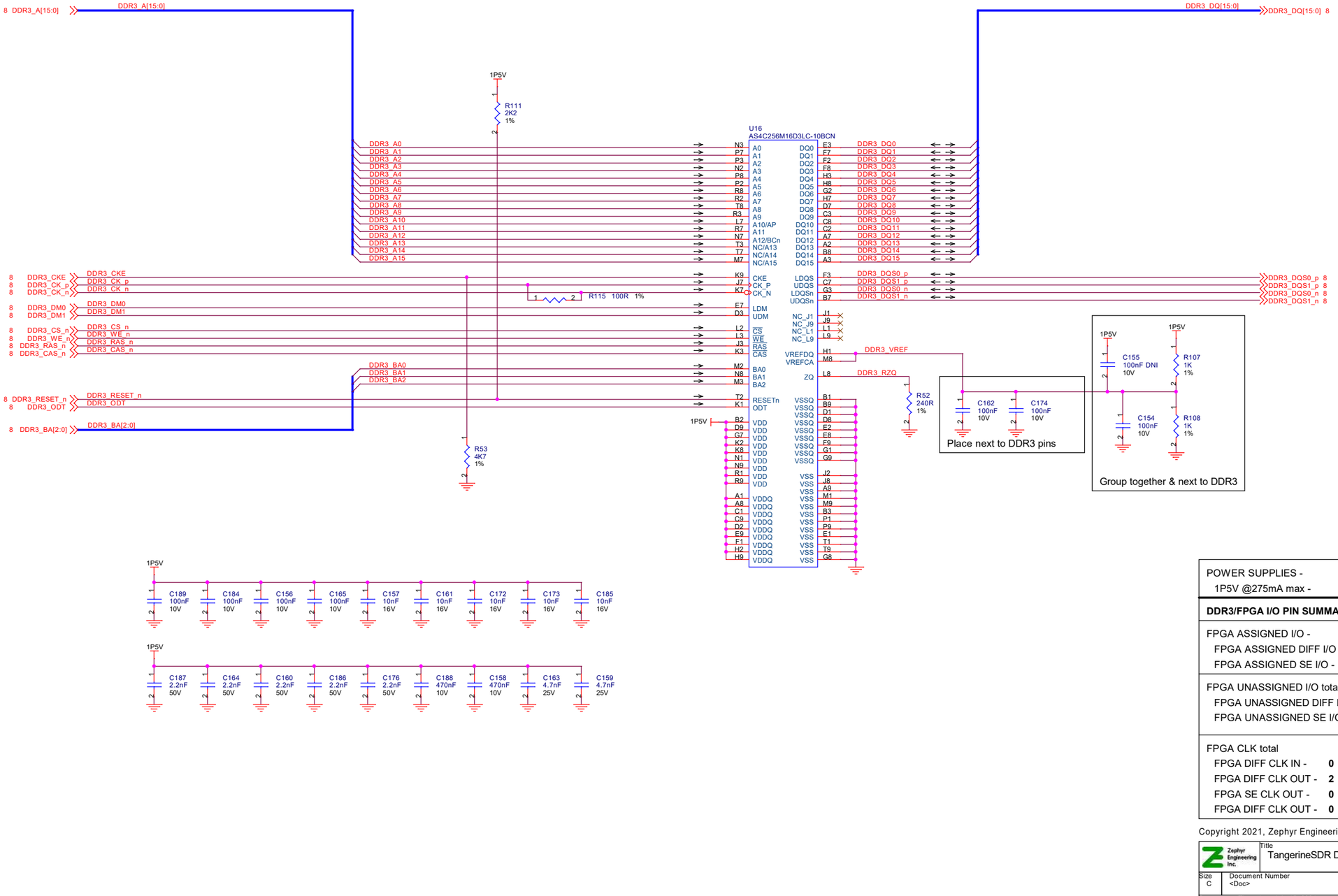

POWER SUPPLIES -	
1P5V @275mA max -	**1**
DDR3/FPGA I/O PIN SUMMARY -	**51**
FPGA ASSIGNED I/O -	**22**
FPGA ASSIGNED DIFF I/O -	**4**
FPGA ASSIGNED SE I/O -	**18**
FPGA UNASSIGNED I/O total	**27**
FPGA UNASSIGNED DIFF I/O -	**0**
FPGA UNASSIGNED SE I/O -	**27**
FPGA CLK total	**2**
FPGA DIFF CLK IN -	**0**
FPGA DIFF CLK OUT -	**2**
FPGA SE CLK OUT -	**0**
FPGA DIFF CLK OUT -	**0**

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Title: TangerineSDR DE DDR3

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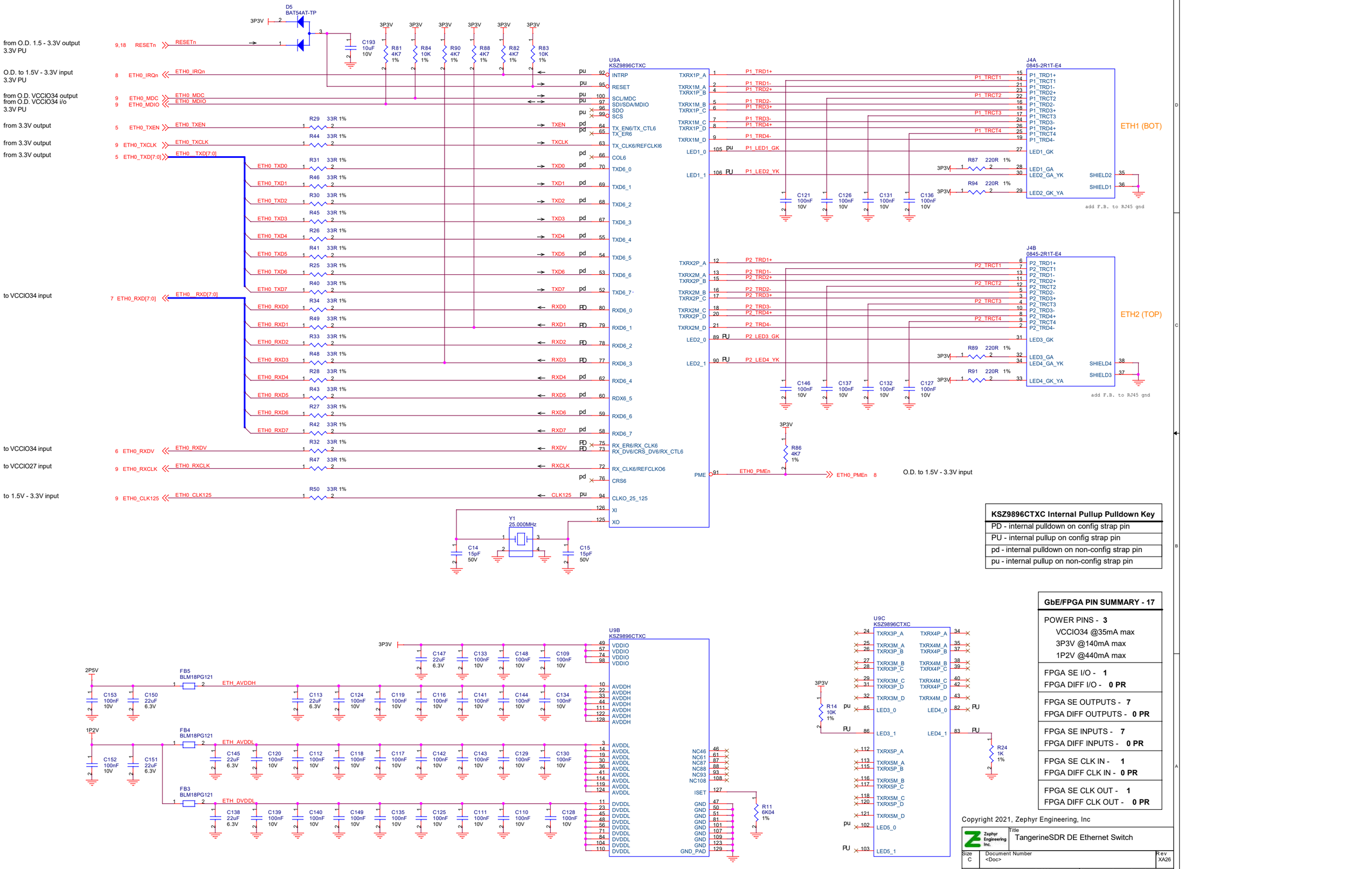

KSZ9896CTXC Internal Pullup Pulldown Key
PD - internal pulldown on config strap pin
PU - internal pullup on config strap pin
pd - internal pulldown on non-config strap pin
pu - internal pullup on non-config strap pin

GbE/FPGA PIN SUMMARY - 17
POWER PINS - **3** VCCIO34 @35mA max 3P3V @140mA max 1P2V @440mA max
FPGA SE I/O - **1** FPGA DIFF I/O - **0 PR**
FPGA SE OUTPUTS - **7** FPGA DIFF OUTPUTS - **0 PR**
FPGA SE INPUTS - **7** FPGA DIFF INPUTS - **0 PR**
FPGA SE CLK IN - **1** FPGA DIFF CLK IN - **0 PR**
FPGA SE CLK OUT - **1** FPGA DIFF CLK OUT - **0 PR**

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Title: TangerineSDR DE Ethernet Switch

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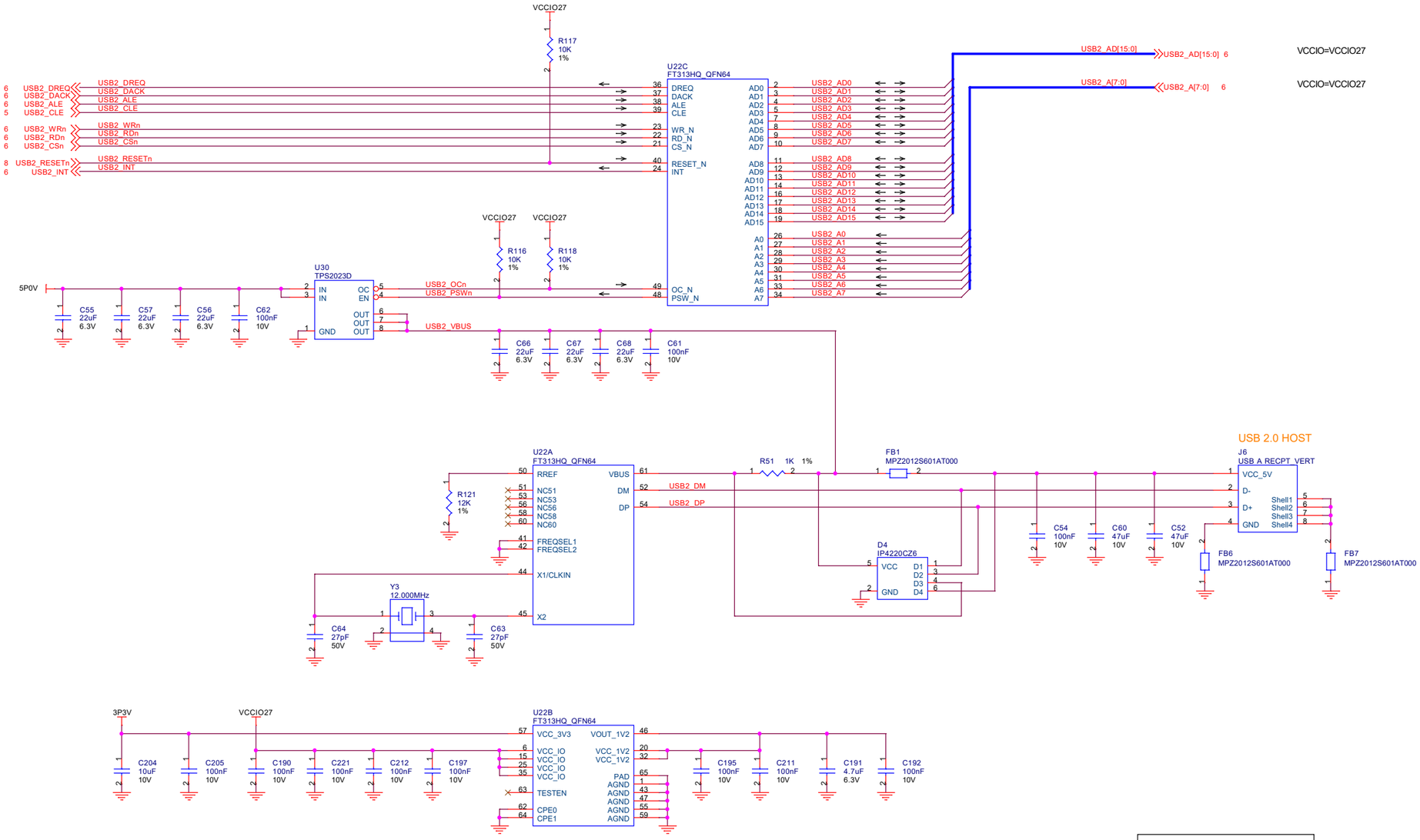
to VCCIO27 input

from VCCIO27 output

from O.D. 1.5 PU VCCIO27 output
to VCCIO27 input



USB2/FPGA PIN SUMMARY - 33
POWER PINS - **1** 3P3V @50mA 5P0V @2.2A
FPGA SE I/O - **16** FPGA DIFF I/O - **0**
FPGA SE OUTPUTS - **15** FPGA DIFF OUTPUTS - **0**
FPGA SE INPUTS - **2** FPGA DIFF INPUTS - **0**
FPGA SE CLK IN - **0** FPGA DIFF CLK IN - **0**
FPGA SE CLK OUT - **0** FPGA DIFF CLK OUT - **0**

Zephyr Engineering Inc.	Title: TangerineSDR DE USB 2.0 Host	
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to 3.3V i/o

5 USB3_BE[3:0] — USB3_BE[3:0]

USB3_BE0 — USB3_BE1 — USB3_BE2 — USB3_BE3

to 3.3V inputs

6 USB3_TXEn — USB3_TXEn

6 USB3_RXFn — USB3_RXFn

from 3.3V outputs

5 USB3_WRn — USB3_WRn

5 USB3_RDn — USB3_RDn

5 USB3_OEn — USB3_OEn

5 USB3_RESETn — USB3_RESETn

U23C
FT601Q

BE_0	4	USB3_BE0
BE_1	5	USB3_BE1
BE_2	6	USB3_BE2
BE_3	7	USB3_BE3
TXE_N	8	USB3_TXEn
RXF_N	9	USB3_RXFn
WR_N	11	USB3_WRn
RD_N	12	USB3_RDn
OE_N	13	USB3_OEn
RESET_N	15	USB3_RESETn
DATA_0	40	USB3_DATA0
DATA_1	41	USB3_DATA1
DATA_2	42	USB3_DATA2
DATA_3	43	USB3_DATA3
DATA_4	44	USB3_DATA4
DATA_5	45	USB3_DATA5
DATA_6	46	USB3_DATA6
DATA_7	47	USB3_DATA7
DATA_8	50	USB3_DATA8
DATA_9	51	USB3_DATA9
DATA_10	52	USB3_DATA10
DATA_11	53	USB3_DATA11
DATA_12	54	USB3_DATA12
DATA_13	55	USB3_DATA13
DATA_14	56	USB3_DATA14
DATA_15	57	USB3_DATA15
DATA_16	60	USB3_DATA16
DATA_17	61	USB3_DATA17
DATA_18	62	USB3_DATA18
DATA_19	63	USB3_DATA19
DATA_20	64	USB3_DATA20
DATA_21	65	USB3_DATA21
DATA_22	66	USB3_DATA22
DATA_23	67	USB3_DATA23
DATA_24	69	USB3_DATA24
DATA_25	70	USB3_DATA25
DATA_26	71	USB3_DATA26
DATA_27	72	USB3_DATA27
DATA_28	73	USB3_DATA28
DATA_29	74	USB3_DATA29
DATA_30	75	USB3_DATA30
DATA_31	76	USB3_DATA31
CLK	58	USB3_CLK

USB3_DATA[31:0] — USB3_DATA[31:0] 5

to 3.3V i/o

USB3_CLK — USB3_CLK 9

to 3.3V input

3P3V — R56 10K 1%

to 1.5V OD w/3.3V PU

8 USB3_WAKEUPn — USB3_WAKEUPn

U23A
FT601Q

SIWU_N	10	
WAKEUP_N	16	USB3_WAKEUPn
GPIO0	17	
GPIO1	18	
NC	19	
XI	21	
XO	22	
RREF	27	
VBUS	37	USB3_VBUS
DM	25	USB3_DM
DP	23	USB3_DP
TODN	31	USB3_SSTX-
TODP	32	USB3_SSTX+
RIDN	34	USB3_SSRX-
RIDP	35	USB3_SSRX+

Y4 30.000MHz

C71 10pF 50V — C70 10pF 50V

R123 1K6 1%

FB8 MPZ2012S601AT000

C75 100nF 10V — C74 100nF 10V

USB 3.0 DEVICE

J9 USB 3.0 microB RA RECPT

VCC_5V	1	
D-	2	
D+	3	
OTG ID	4	
GND	5	
SSTX-	6	
SSTX+	7	
GND	8	
SSRX-	9	
SSRX+	10	
Shell1	11	
Shell2	12	

FB9 MPZ2012S601AT000

FB11 MPZ2012S601AT000

D1 ESD7016

I/O1	1	
I/O2	2	
VBUS/GND	3	
I/O3	4	
I/O4	5	
GND	6	
I/O5	7	
I/O6	8	
NC	10	
NC	9	

C201 100nF 10V

3P3V

C245 10uF 10V — C199 100nF 10V — C200 100nF 10V — C207 100nF 10V

C223 100nF 10V — C263 100nF 10V — C259 100nF 10V — C246 100nF 10V — C222 100nF 10V

U23B
FT601Q

VCC33	20	
VCC33	24	
VCC33	38	
VDDA	28	
VCCIO	14	
VCCIO	49	
VCCIO	59	
VCCIO	68	
PAD	77	
DV10	39	
VD10	3	
VD10	30	
VD10	33	
VD10	48	
AVDD	2	
GND	1	
GND	26	
GND	29	
GND	36	

C260 100nF 10V

C198 100nF 10V — C206 100nF 10V — C239 100nF 10V — C240 100nF 10V — C262 4.7uF 6.3V — C261 100nF 10V

USB3/FPGA PIN SUMMARY - 46
POWER PINS - **1** 3P3V @275mA
FPGA SE I/O - **39** FPGA DIFF I/O - **0**
FPGA SE OUTPUTS - **4** FPGA DIFF OUTPUTS - **0**
FPGA SE INPUTS - **2** FPGA DIFF INPUTS - **0**
FPGA SE CLK IN - **1** FPGA DIFF CLK IN - **0**
FPGA SE CLK OUT - **0** FPGA DIFF CLK OUT - **0**

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Title: TangerineSDR DE USB 3.0 Host

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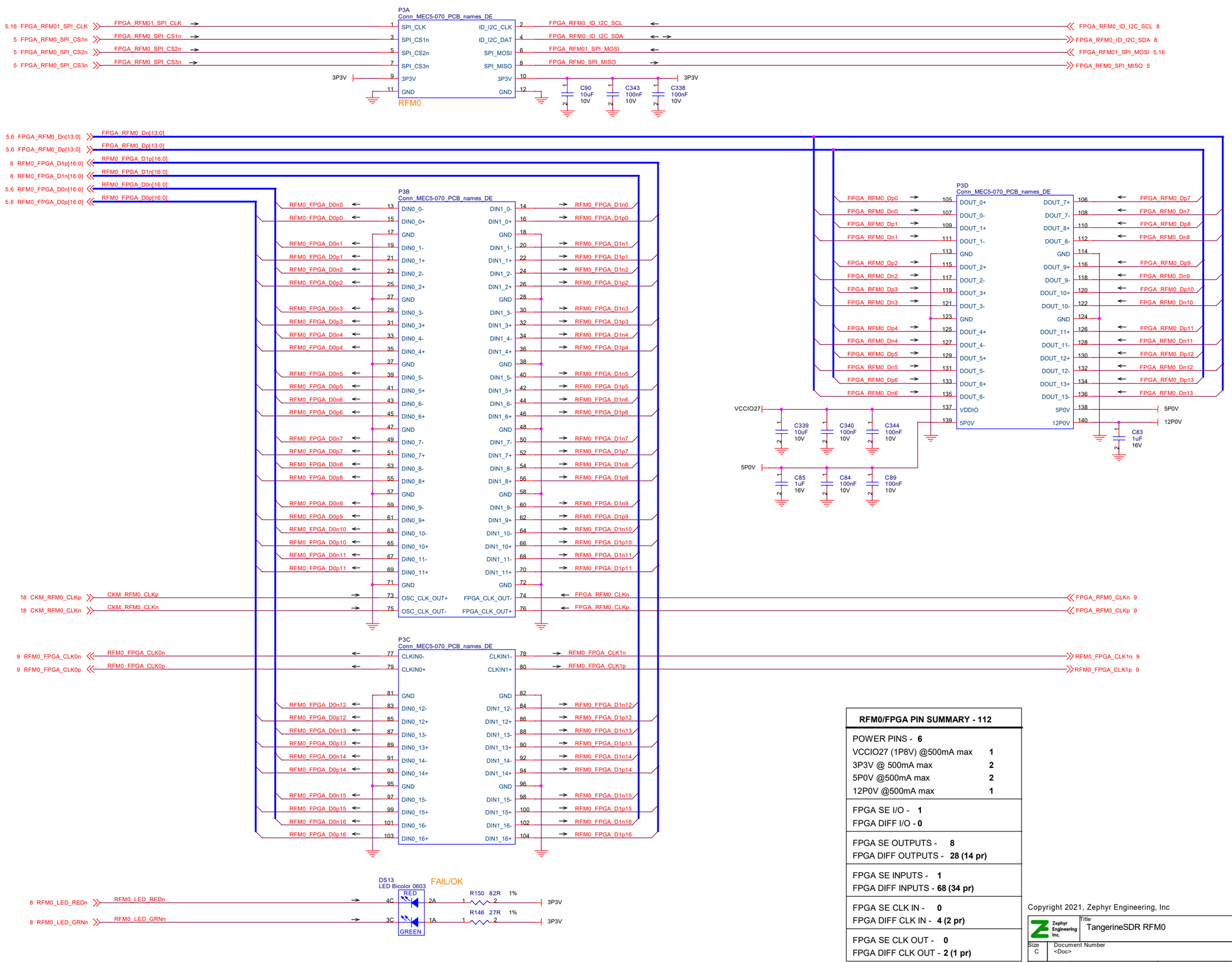

RFM0/FPGA PIN SUMMARY - 112	
POWER PINS - **6**	
VCCIO27 (1P8V) @500mA max	**1**
3P3V @ 500mA max	**2**
5P0V @500mA max	**2**
12P0V @500mA max	**1**
FPGA SE I/O - **1**	
FPGA DIFF I/O - **0**	
FPGA SE OUTPUTS - **8**	
FPGA DIFF OUTPUTS - **28 (14 pr)**	
FPGA SE INPUTS - **1**	
FPGA DIFF INPUTS - **68 (34 pr)**	
FPGA SE CLK IN - **0**	
FPGA DIFF CLK IN - **4 (2 pr)**	
FPGA SE CLK OUT - **0**	
FPGA DIFF CLK OUT - **2 (1 pr)**	

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Title: TangerineSDR RFM0

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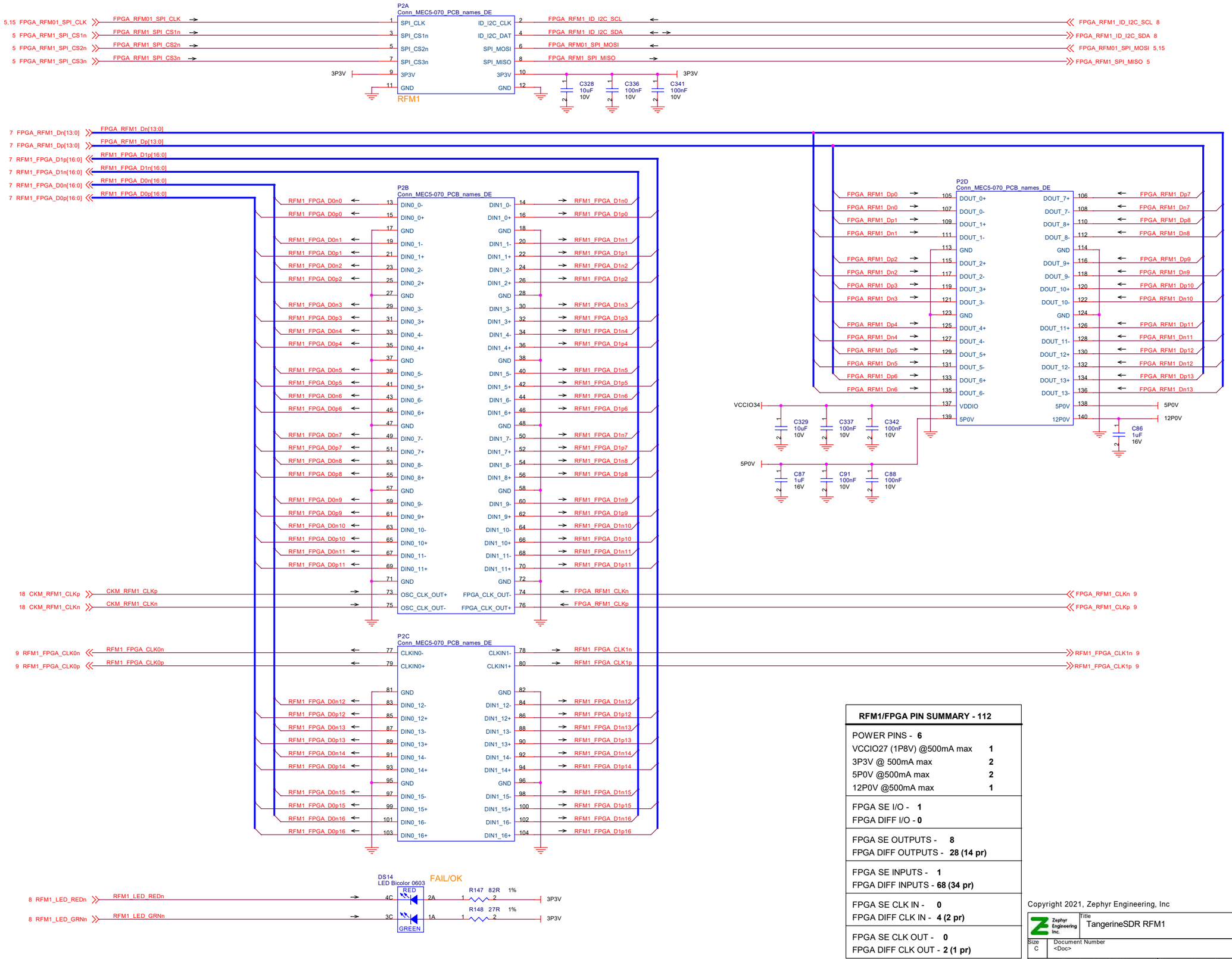

RFM1/FPGA PIN SUMMARY - 112

POWER PINS - **6**	
VCCIO27 (1P8V) @500mA max	**1**
3P3V @ 500mA max	**2**
5P0V @500mA max	**2**
12P0V @500mA max	**1**
FPGA SE I/O - **1**	
FPGA DIFF I/O - **0**	
FPGA SE OUTPUTS - **8**	
FPGA DIFF OUTPUTS - **28 (14 pr)**	
FPGA SE INPUTS - **1**	
FPGA DIFF INPUTS - **68 (34 pr)**	
FPGA SE CLK IN - **0**	
FPGA DIFF CLK IN - **4 (2 pr)**	
FPGA SE CLK OUT - **0**	
FPGA DIFF CLK OUT - **2 (1 pr)**	

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Title: TangerineSDR RFM1

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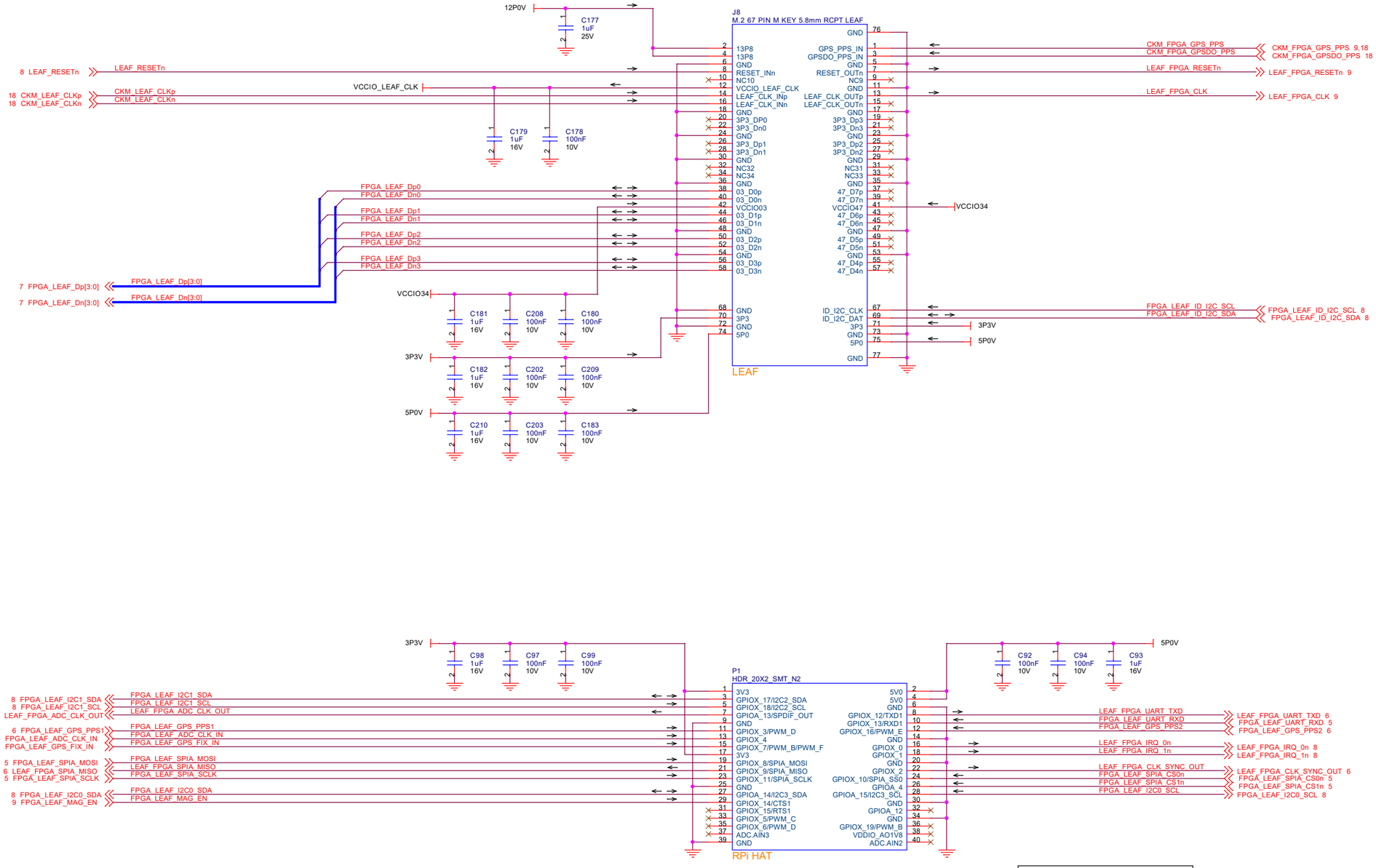

LEAF/FPGA PIN SUMMARY - 44	
POWER PINS - **4**	
3P3V @100mA max	
5P0V @700mA max	
12P0V @100mA max	
VCCIO27 @100mA max	
FPGA SE I/O - **4**	
FPGA DIFF I/O - **15**	
FPGA SE OUTPUTS - **17**	
FPGA DIFF OUTPUTS - **0**	
FPGA SE INPUTS - **8**	
FPGA DIFF INPUTS - **0**	
FPGA SE CLK IN - **0**	
FPGA DIFF CLK IN - **0**	
FPGA SE CLK OUT - **0**	
FPGA DIFF CLK OUT - **0**	

Zephyr Engineering Inc.	Title: TangerineSDR LEAF Interface	
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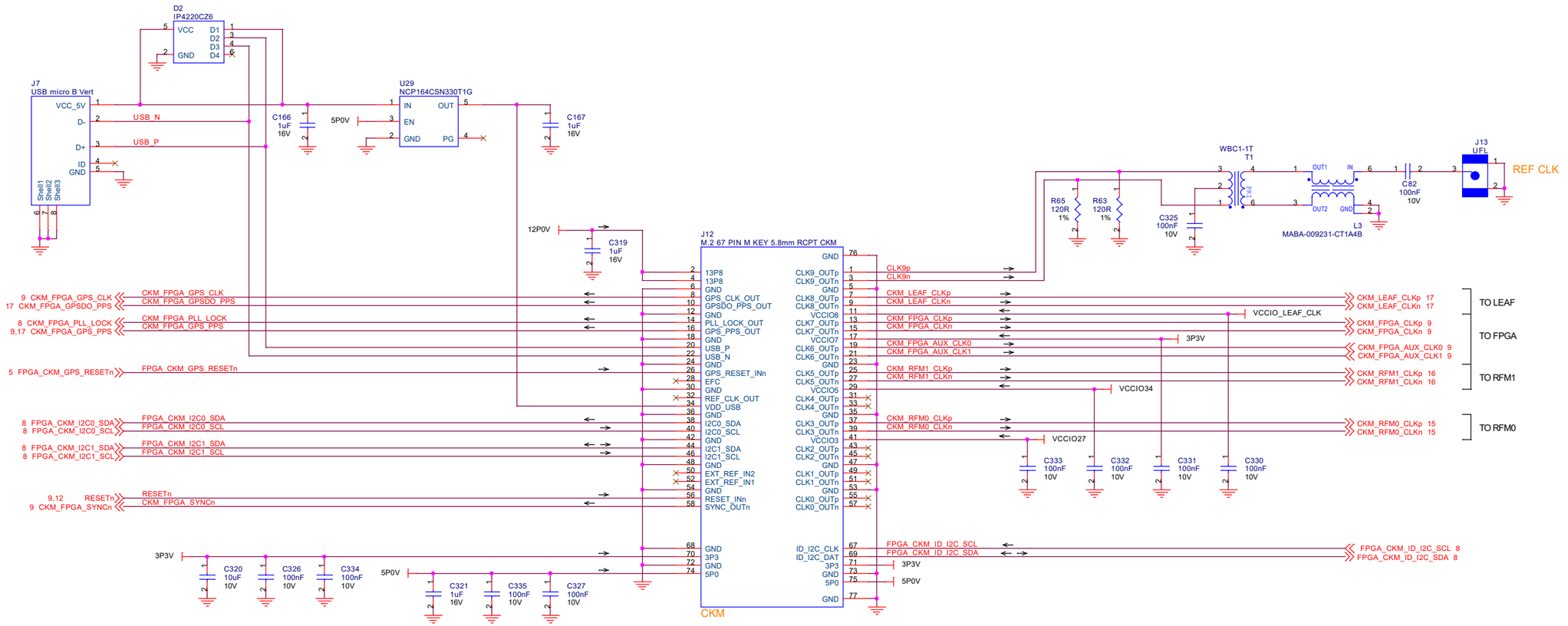

CKM/FPGA PIN SUMMARY - 16
POWER PINS - **6** 3P3V @100mA max 5P0V @200mA max 12P0V @1A max VCCIO27 @100mA VCCIO34 @100mA VCCIO_LEAF_CLK @ 100mA
FPGA SE I/O - **3** FPGA DIFF I/O - **0 PR**
FPGA SE OUTPUTS - **7** FPGA DIFF OUTPUTS - **0 PR**
FPGA SE INPUTS - **5** FPGA DIFF INPUTS - **0 PR**
FPGA SE CLK IN - **2** FPGA DIFF CLK IN - **1 PR**
FPGA SE CLK OUT - **0** FPGA DIFF CLK OUT - **0 PR**

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1.5V FPGA I/O OD
1.5V FPGA OUT OD
3.3V FPGA OUT

8 LOCAL_I2C_SDA
8 LOCAL_I2C_SCL
9 LOCAL_I2C_WEn

LOCAL_I2C_SDA
LOCAL_I2C_SCL
LOCAL_I2C_WEn

1.7 to 5.5V

U17
M24512-DFMC6TG
SDA
SCL
WC
E0
E1
E3
VCC
PAD
GND
1.7 to 5.5V
3P3V
C171
100nF
10V

M24512 512K-bit EEPROM I2C ADDRESSES

MEM ARRAY	1	0	1	0	0	0	0	RW
ID PAGE	1	0	1	1	0	0	0	RW

1.8 to 5.5V

U18
ATECC608A-MAHDA-S
SDA
SCL
NC1
NC2
NC3
NC7
VCC
PAD
GND
2.0 to 5.5V
3P3V
C170
100nF
10V

ATECC508A CRYPTO CHIP I2C ADDRESS

1	1	0	0	0	0	0	RW

1.7 to 5.5V

U19
AT30TS74-MA8M
SDA
SCL
A0
A1
A2
VDD
ALERT
PAD
GND
1.7 to 5.5V
3P3V
C169
100nF
10V

AT30TS74 TEMPERATURE SENSOR I2C ADDRESS

1	0	0	1	0	0	0	RW

1P5V
R114
2K2
1%
I2C_OTEMPn
I2C_OTEMPn 8

1.8 to 5.5V

U15
PCF8563TS/5
SDA
SCL
OSCI
OSCO
VDD
CLKOUT
INT
VSS
RTC_VDD
C168
100nF
10V
BAT_POS
3P3V
D3
BAT54CT
CR1216_SKT
BT1
Y2
32.768kHz
PAD
C49
10pF
50V
C47
10pF - DNI
50V
3P3V
R110
4K7
1%
1P5V
R104
2K2
1%
TP9
Test Point
RTC
RTC_CLKOUT
RTC_CLKOUT 8
RTC_INTn
RTC_INTn 8

PCF8563 REAL TIME CLOCK I2C ADDRESS

1	0	0	1	0	0	0	RW

1.5V FPGA IN

3.3V FPGA I/O

3P3V
R64
4K7
1%
R145
4K7
1%
R144
4K7
1%
R68
4K7
1%

5 QSPI_CLK
5 QSPI_DQ[3:0]
5 QSPI_CSn

QSPI_CLK
QSPI_DQ[3:0]
QSPI_DQ0
QSPI_DQ1
QSPI_DQ2
QSPI_DQ3
QSPI_CSn

U28
MT25QL512ABB1EW9-0SIT
CLK
nCS
DQ0
DQ1
W#/DQ2
HOLD#/DQ3
VCC
VSS
PAD
3P3V
C324
100nF
10V

I2C FPGA PIN SUMMARY - 6

POWER PINS - **2**
3P3V @ 10mA
1P5V @ 2mA

FPGA SE I/O - **1 @ 1.5V OD**

FPGA SE OUTPUTS - **1 @ 1.5V OD**
FPGA SE OUTPUTS - **1 @ 3.3V**

FPGA SE INPUTS - **3 (@ 1.5V**

QSPI FPGA PIN SUMMARY - 6

POWER PINS - **1**
3P3V @40mA

FPGA SE I/O - **4 @ 3.3V**
FPGA SE OUTPUTS - **2 @ 3.3V**

Zephyr Engineering Inc.

Title: TangerineSDR QSPI, I2C

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VCC_SD
1.8V/3.3V@600mA

1.5V FPGA I/O
OPEN DRAIN

SD_1P8V_SEL = 1 FOR 1.8V SIGNALLING
SD_1P8V_SEL = 0 FOR 3.3V SIGNALLING

SLEW RATE LIMIT
THESE I/O PINS

1.5V FPGA I/O
TOTEM POLE

uSDC FPGA PIN SUMMARY - 11

POWER PINS -	**3**
1P5V @10mA	
3P3V @200mA	
5P0V @100mA	
FPGA SE I/O -	**5 @ 1.5V**
FPGA SE OUTPUTS -	**2 @ 1.5V**
FPGA SE OUTPUTS -	**2 @ 1.5V OD**
FPGA SE INPUTS -	**2 @ 1.5.V**

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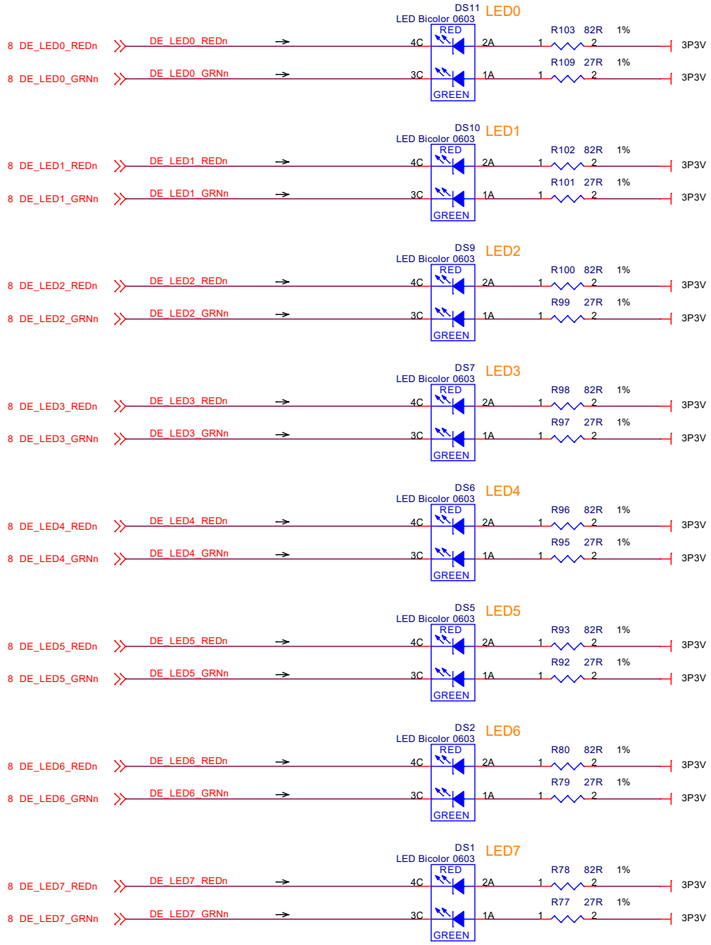
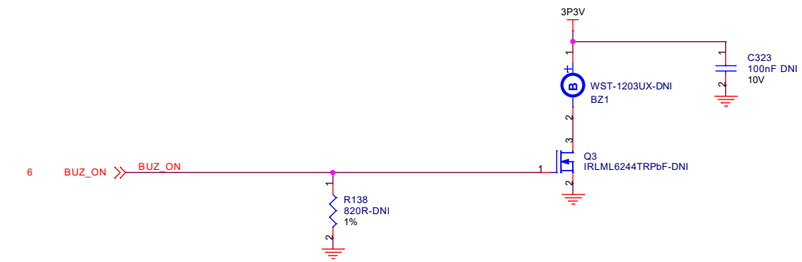
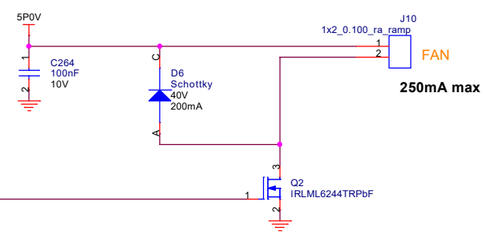
1.5V FPGA I/O
OPEN DRAIN



VCCIO27 FPGA I/O
TOTEM POLE





1.5V FPGA I/O
TOTEM POLE

FPGA PIN SUMMARY - 18

POWER PINS - **1**
3P3V @320mA max
5P0V @100mA max

FPGA Output - **17 @ 1.5V OD**
FPGA Output - **1 @ VCCIO27**

Zephyr Engineering Inc.

Title: TangerineSDR LED_BUZ_FAN

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12P0V
11-15V@4A
POWER INPUT

Powerup sequence:
12V-->5V-->3.3V-->1.5V-->VCCIO27/VCCIO34-->1.2V

5P0V
5.0V@6A

J1
5.5x2.5mm
PWR IN
VIN
L1
DLW5ATZ450TQ2L
12P0V
C95 100nF 25V
C5 22uF 25V
C6 22uF 25V
C96 100nF 25V
C4 10nF 16V
U1
TPS65286
VIN
EN
SS
SW_EN1
SW_EN2
COMP
RLIM
RSET1
RSET2
MODE/SYNC
VTV
AGND
GND
PAD
LX
BST
FB
nFAULT1
nFAULT2
SW_IN1
SW_IN2
SW_OUT1
SW_OUT2
R6 10K 1%
C2 10pF 50V
C1 2.2nF 50V
R5 169K 1%
R4 15K 1%
R3 15K 1%
C8 1uF 16V
L2 4.7uH
C7 47nF 25V
C3 82pF 50V
R1 39K2 1%
R2 5K36 1%
5P0V_FB
VFB=0.6V
TP1
Test Point
5P0V
C10 47uF 10V
C9 47uF 10V
C11 47uF 10V
C12 47uF 10V
C13 100nF 10V

3P3V
3.3V@4A

5P0V
U12
EN6347QI
PVIN
AVIN
ENABLE
SS
AGND
LLM/SYNC
PGND
PGND(pad)
VOUT
VFB
POK
RLLM
NC(SW)
NC
C32 22uF 25V
C28 100nF 10V
C27 47uF 10V
C36 47uF 10V
C39 1uF 16V
C46 100nF 10V
TP8
Test Point
3P3V
3P3V_VFB
VFB=0.75V
IFB=5nA
R22 200K 1%
R23 59K 1%
C21 22pF 50V
R85 100K 1%
3P3V_POK
TP4
Test Point
3P3V_POK
3P3V_POK 24
Green
DS4
3.3V PWR
R21 100R 1%
C22 15nF 16V
RAMP TIME = 1.2mS
AUTO LLM MODE

1P2V
1.2V@4A

U11
EN6347QI
5P0V
C31 22uF 25V
C26 100nF 10V
R12 100K 1%
23 VCCIO2347_POK
VCCIO2347_POK
C25 47uF 10V
C35 47uF 10V
C38 1uF 16V
C45 100nF 10V
TP7
Test Point
1P2V
1P2V
1P2V_VFB
VFB=0.75V
IFB=5nA
R19 200K 1%
R20 332K 1%
C19 39pF 50V
R13 100K 1%
1P2V_POK
TP3
Test Point
1P2V_POK
C20 15nF 16V
RAMP TIME = 1.2mS
AUTO LLM MODE

MH1 4-40 Plt Hole
MH2 4-40 Plt Hole
MH3 4-40 Plt Hole
MH4 4-40 Plt Hole
MH5 4-40 Plt Hole
MH6 4-40 Plt Hole
MH7 4-40 Plt Hole
MH8 4-40 Plt Hole
MH9 #2 Plt Hole

Zephyr Engineering Inc.

Title: TangerineSDR Power Supply, 5V, 3.3V, 1.2V

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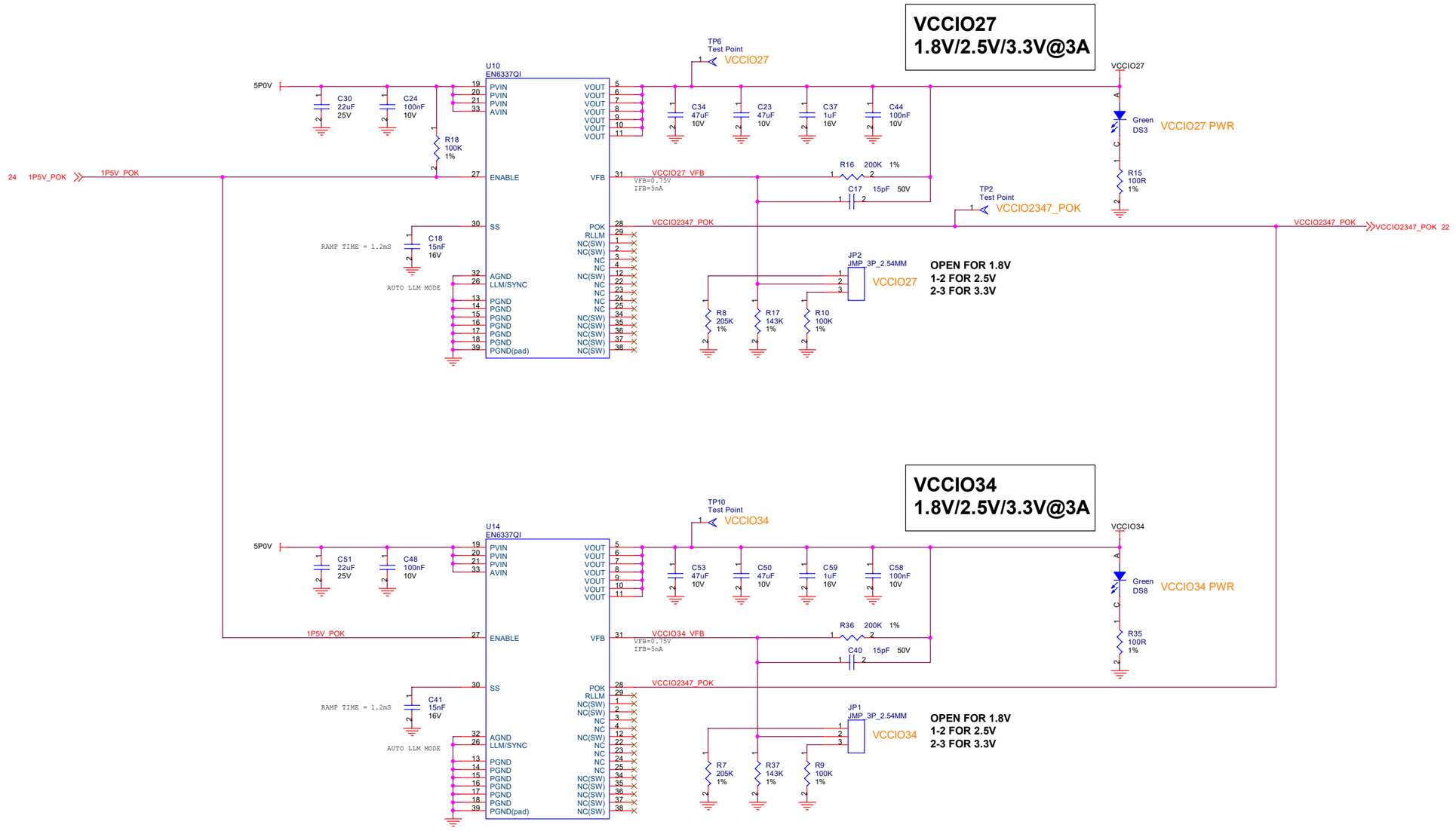
Powerup sequence:
12V-->5V-->3.3V-->1.5V-->VCCIO27/VCCIO34-->1.2V



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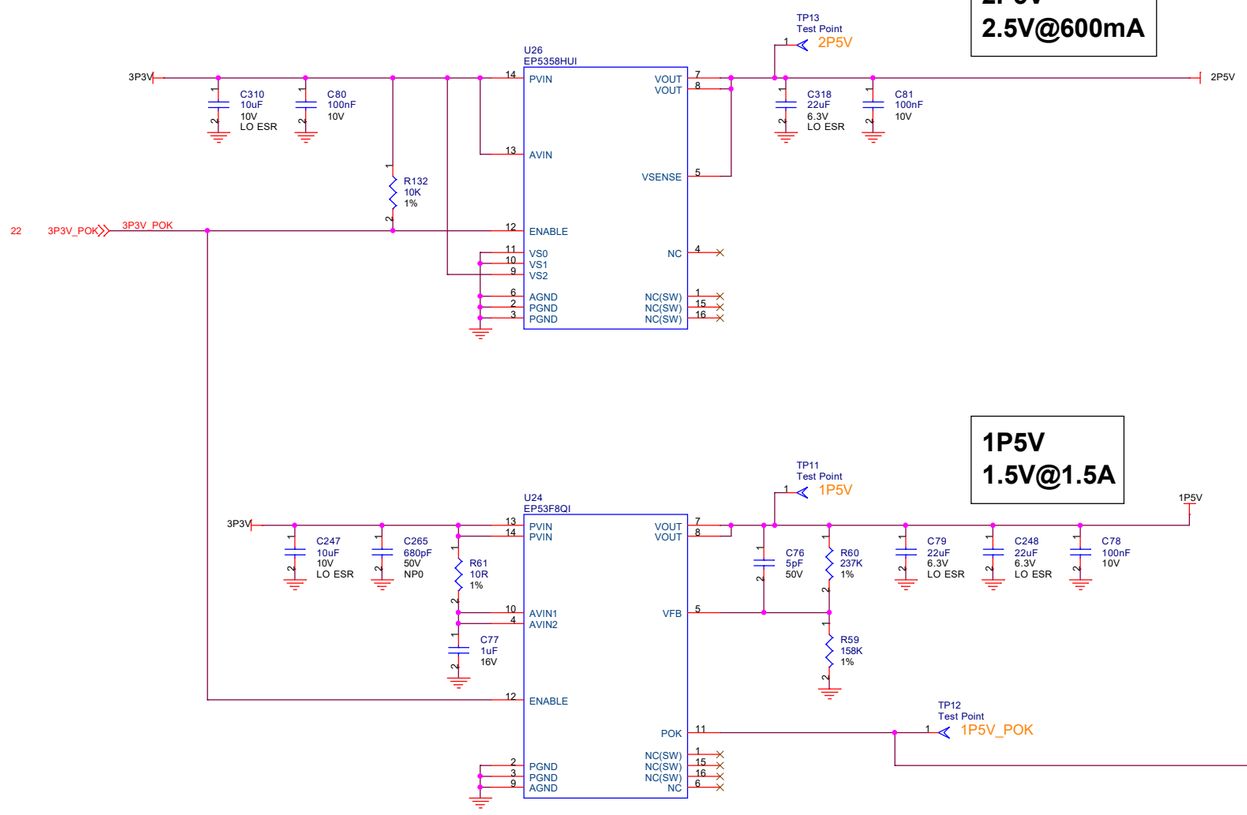
Powerup sequence:
12V-->5V-->3.3V-->1.5V-->VCCIO27/VCCIO34-->1.2V

2P5V
2.5V@600mA



1P5V
1.5V@1.5A

Zephyr Engineering Inc.	Title: TangerineSDR Power Supply, 2.5V, 1.5V	
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