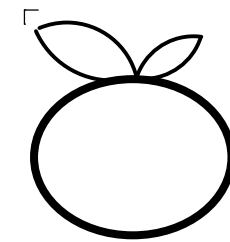



Rev	Date	Name	Description
XA1	20Aug2021	WA2DFI	Original drawing
XA2	12Jan2022	WA2DFI	Connector pin name updates, add MICTOR
XA3	27Mar2022	WA2DFI	Library cleanup
XA4	28Mar2022	WA2DFI	Change display
XA5	31Mar2022	WA2DFI	Add bypass caps
XA6	31Mar2022	WA2DFI	Fix typos
XA7	11Apr2022	WA2DFI	Swap diff pair p/n
XA8	11Apr2022	WA2DFI	Missed one swap
XA9	13Apr2022	WA2DFI	Add GND pins to I2C headers
A	18Apr2022	WA2DFI	Release to Rev A prototype, no changes

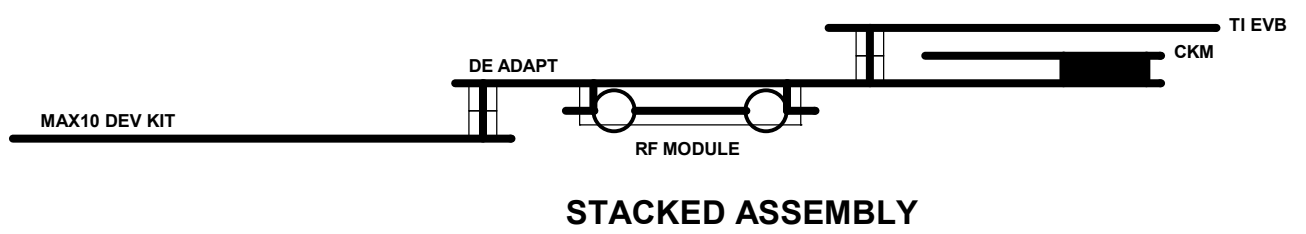
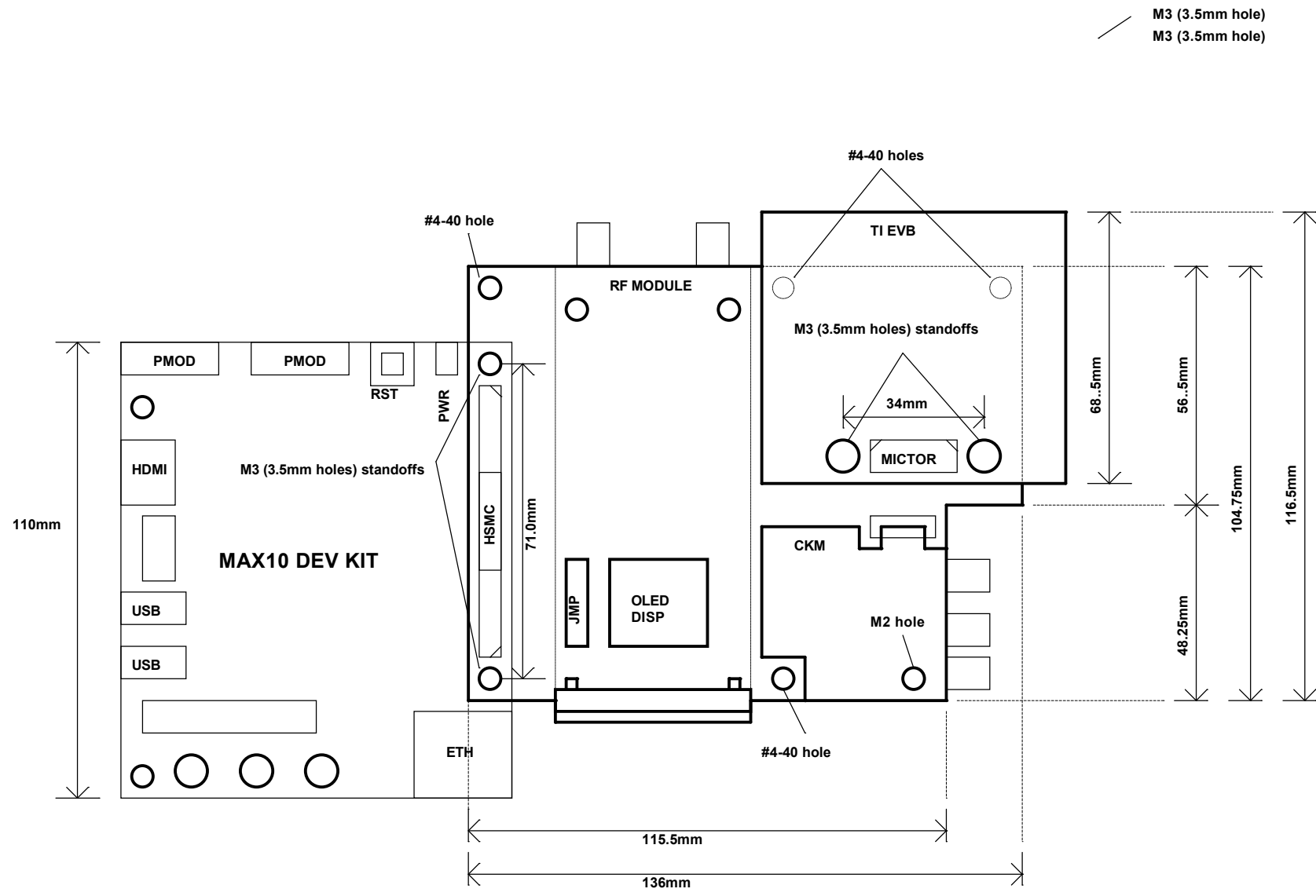
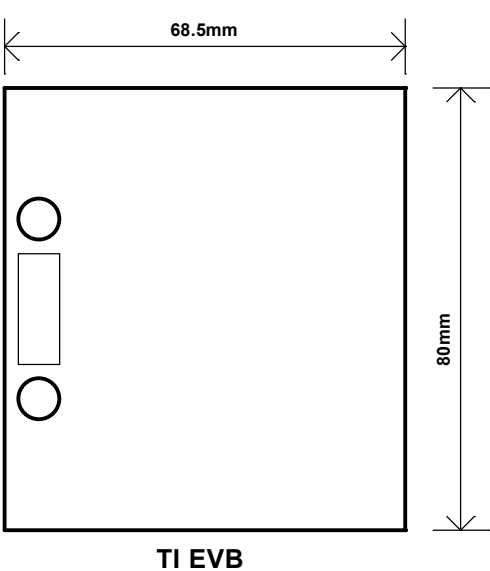
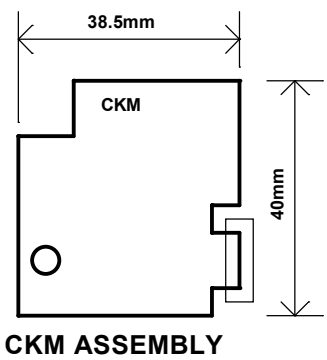
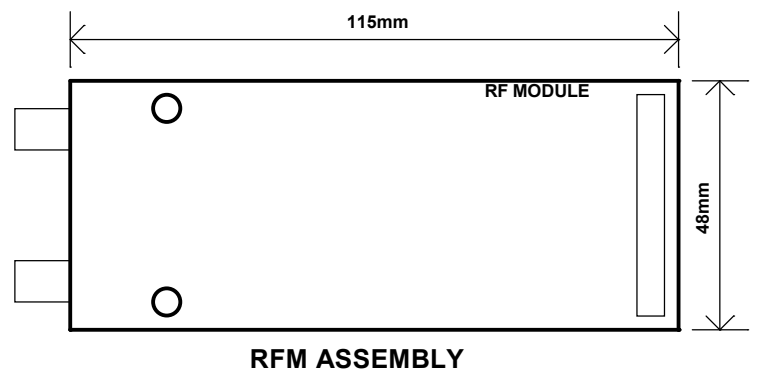
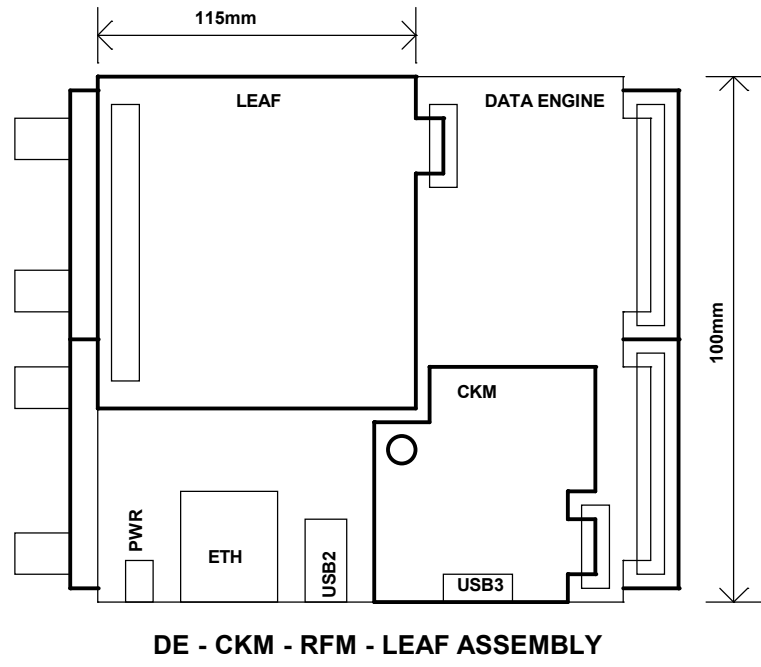
Pg	Contents
1	Cover
2	Layout
3	HSMC connector
4	RFM connector
5	CKM connector
6	MICTOR connector
7	Display and Jumpers
8	Power Supplies

COMPL
X
X
X
X
X
X
X
X



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M3 (3.5mm hole)
M3 (3.5mm hole)

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Z Zephyr Engineering Inc.	Title TangerineSDR DE Adapter Layout	
	Size C	Document Number <Doc>
Date: Monday, April 18, 2022	Sheet 2 of 8	Rev A

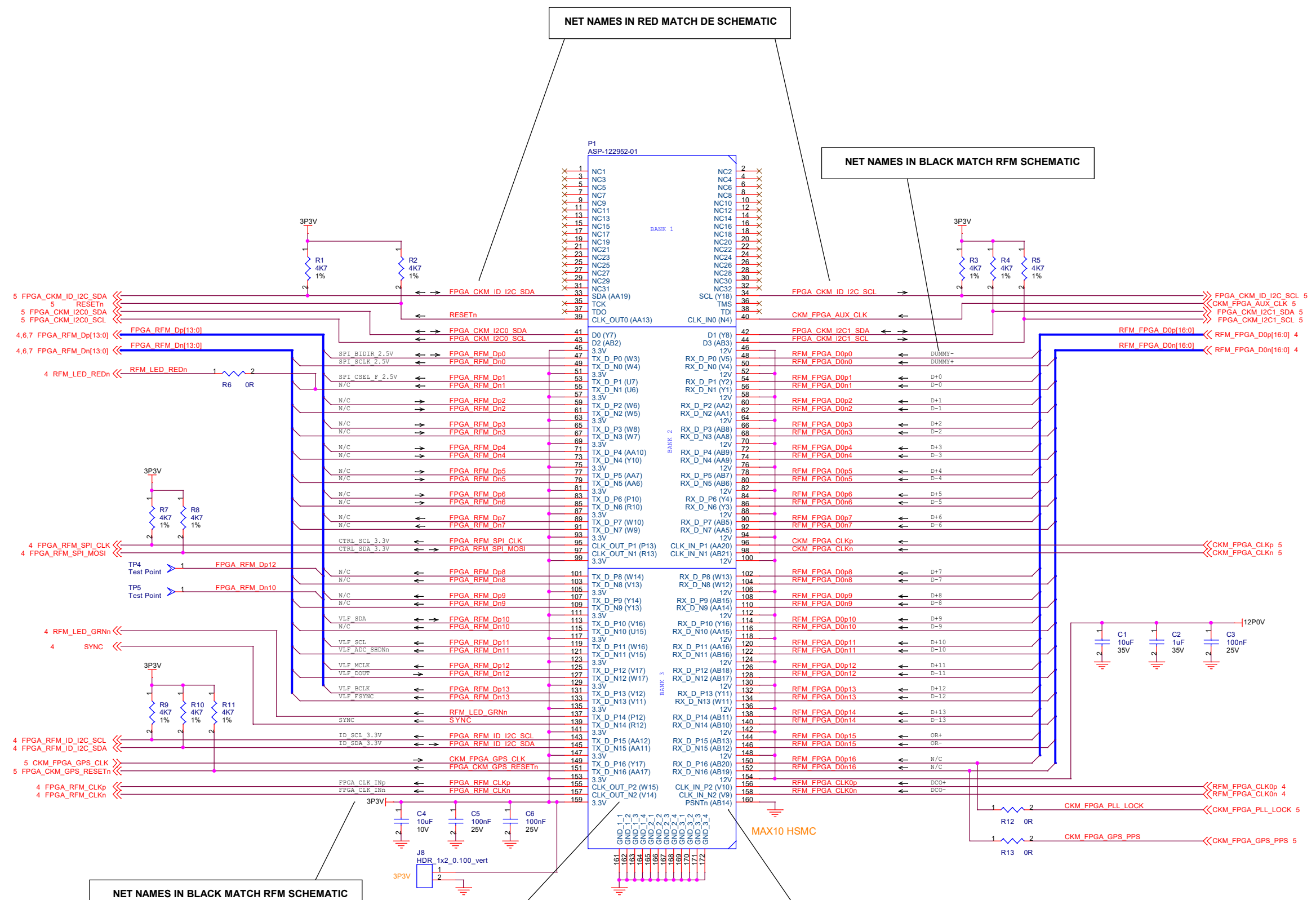
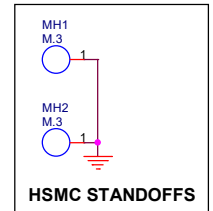
NET NAMES IN RED MATCH DE SCHEMATIC

NET NAMES IN BLACK MATCH RFM SCHEMATIC

NET NAMES IN BLACK MATCH RFM SCHEMATIC

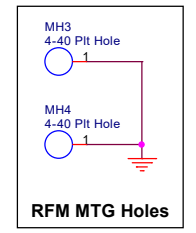
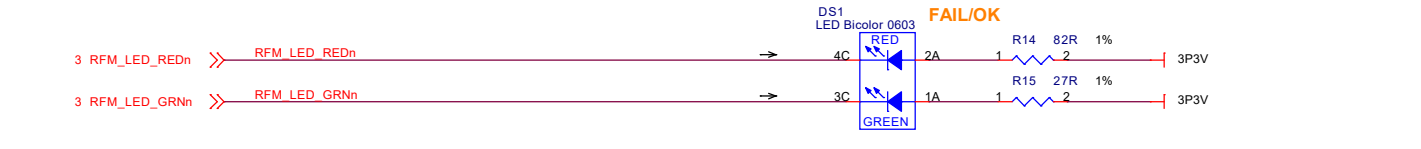
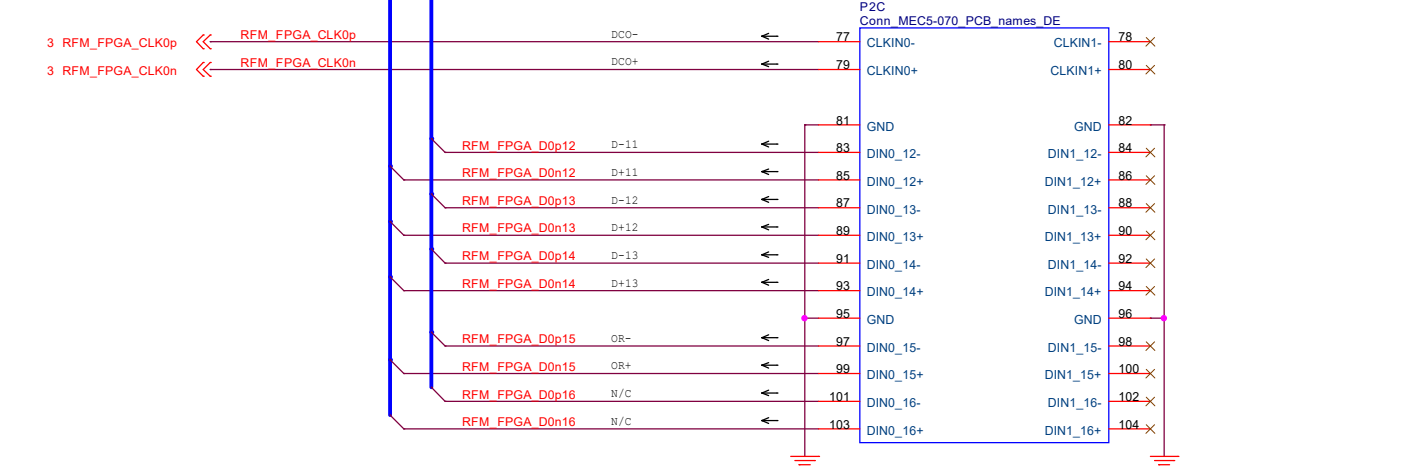
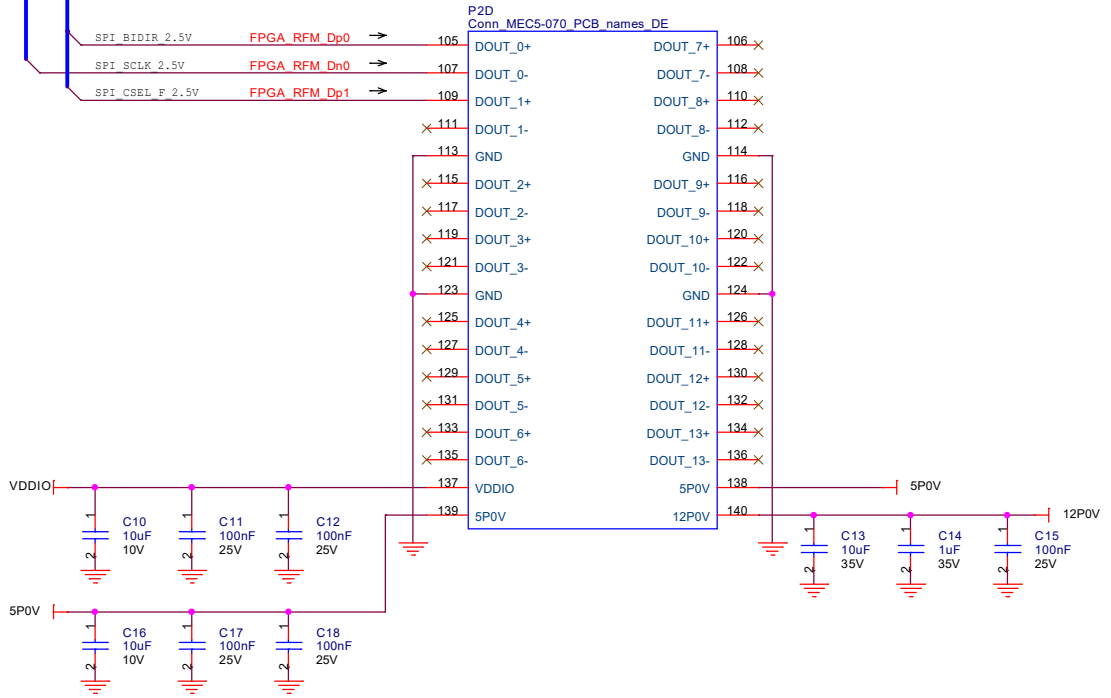
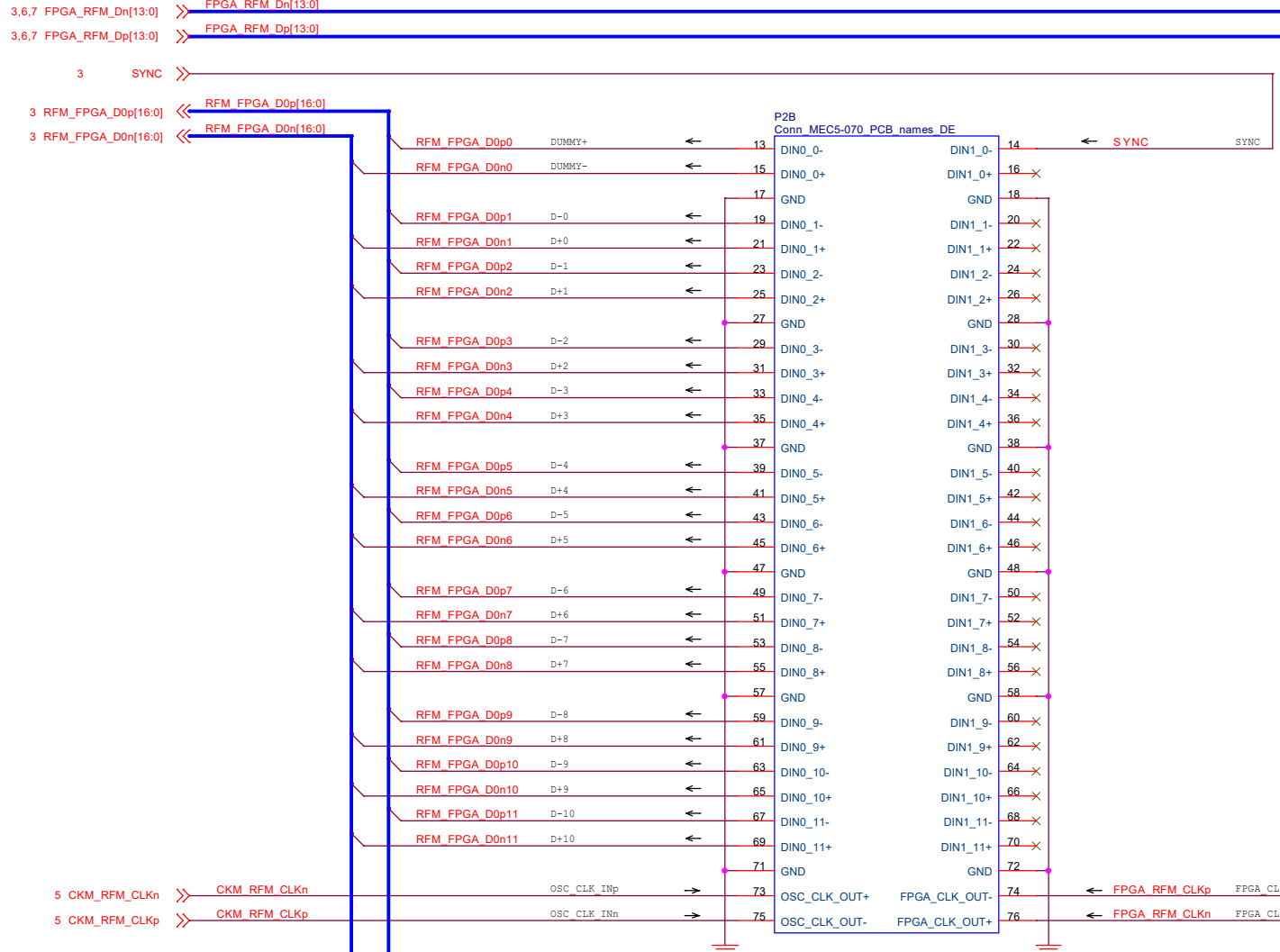
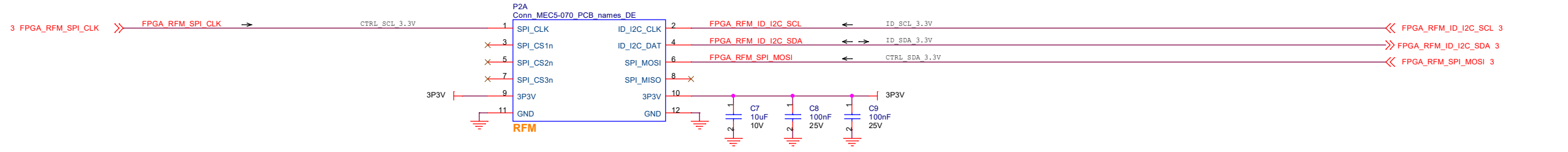
P1 CONNECTOR PIN NAMES ARE J2 CONNECTOR PIN NAMES THAT MATCH MAX10 DEV KIT 6XX-44292R

P1 CONNECTOR PIN NAMES IN (PARENS) ARE FPGA (U1) PIN NUMBERS THAT MATCH MAX10 DEV KIT 6XX-44292R



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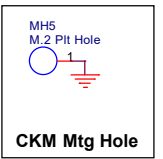
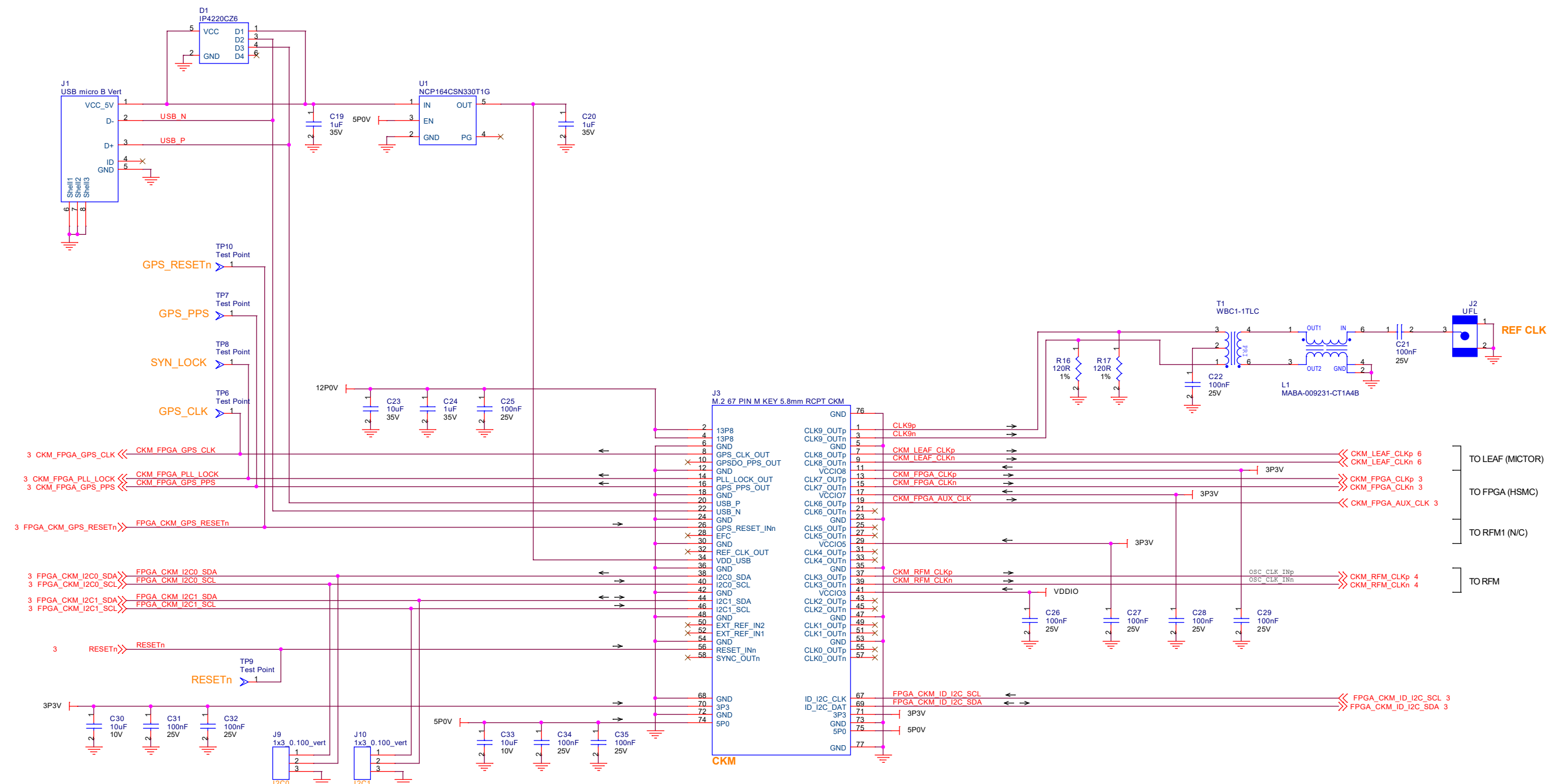
		Title TangerineSDR DE Adapter HSMC connector	
Size C	Document Number <Doc>	Date: Monday, April 18, 2022	Rev A
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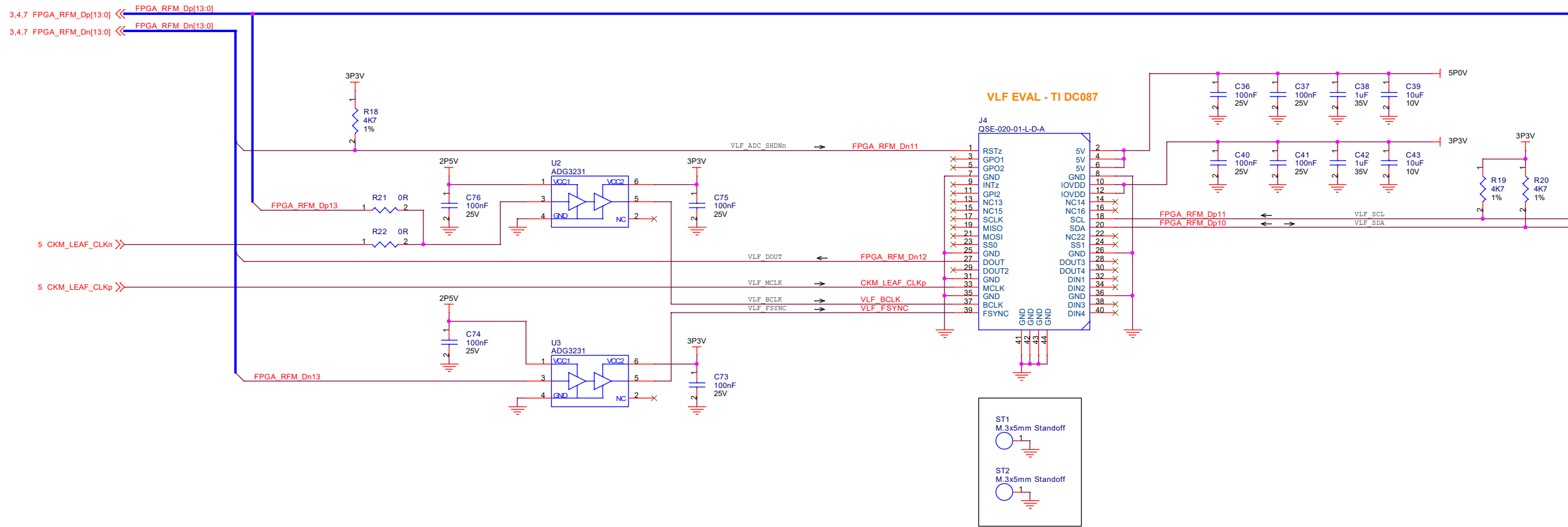
RFM Power Req	
VDDIO_RFM @ 10mA	
3P3V @ 181mA	
5P0V @ 395mA	
12P0V @ 10mA	

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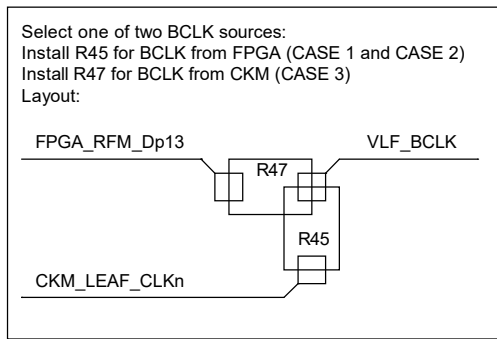
Z Zephyr Engineering Inc.	Title	
	TangerineSDR DE Adapter RFM connector	
Size C	Document Number <Doc>	Rev A
Date: Monday, April 18, 2022	Sheet 4	of 8



CKM Power Req		Copyright 2022, TAPR, Inc Licensed under OHL - https://tapr.org/OHL Design by WA2DFI	
3P3V @ 286mA		Zephyr Engineering Inc.	Title TangerineSDR DE Adapter CKM connector
5P0V @ 408mA			Size C Document Number <Doc> Rev A
12P0V @ 0mA		Date: Monday, April 18, 2022	Sheet 5 of 8



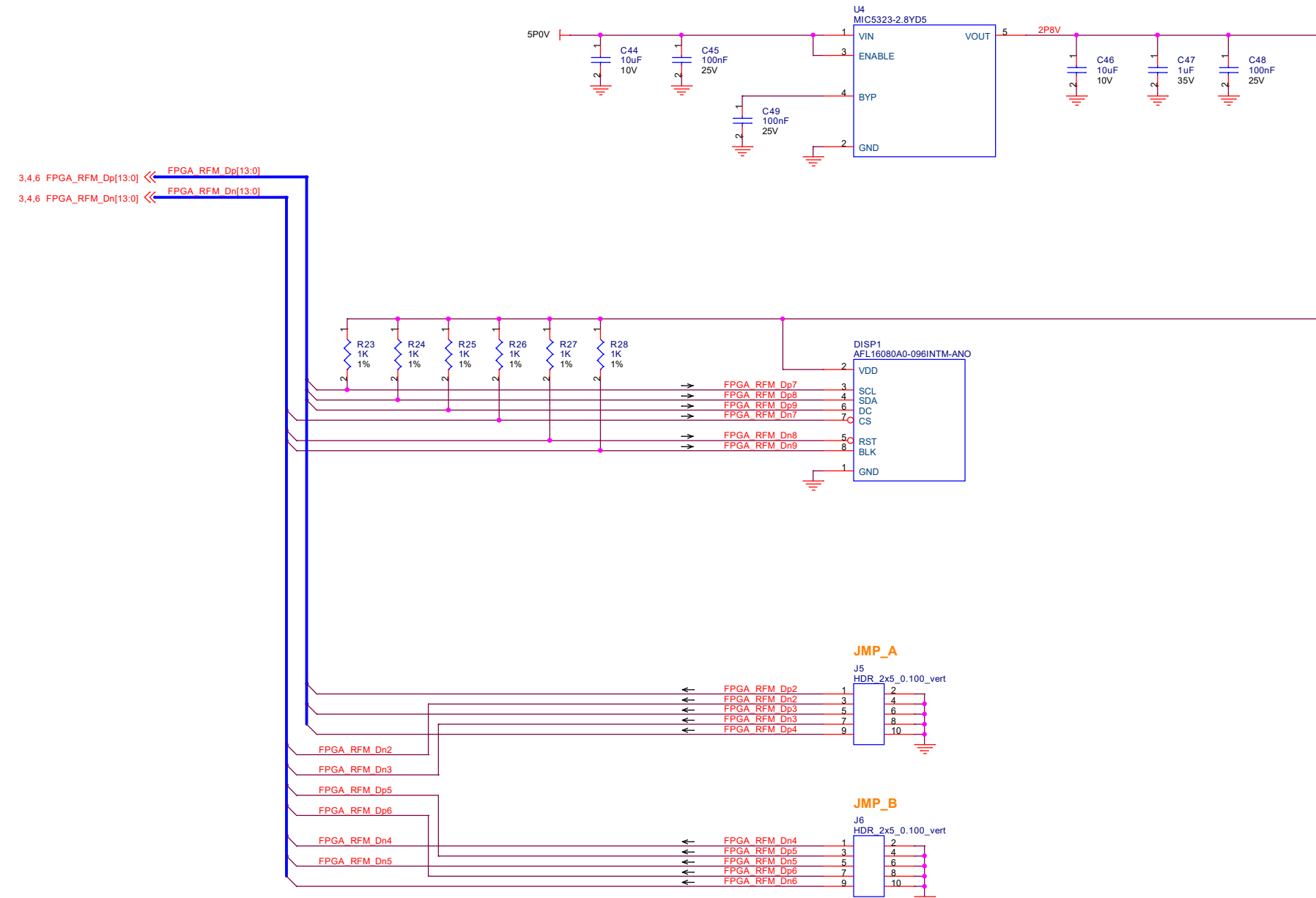
PLACE STANDOFFS ON MICTOR C/L xx mm apart



CLOCK CASES
CASE 1 (DEFAULT): MCLK from CKM BCLK from FPGA
CASE 2: MCLK ground (J13 on ADC EVM) BCLK from FPGA
CASE 3: MCLK ground (J13 on ADC EVM) BCLK from CKM

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VLF Power Req 3P3V @ 20mA 5P0V @ 50mA		Title TangerineSDR DE Adapter VLFconnector	
		Size C	Document Number <Doc>
Date: Monday, April 18, 2022		Sheet 6 of 8	

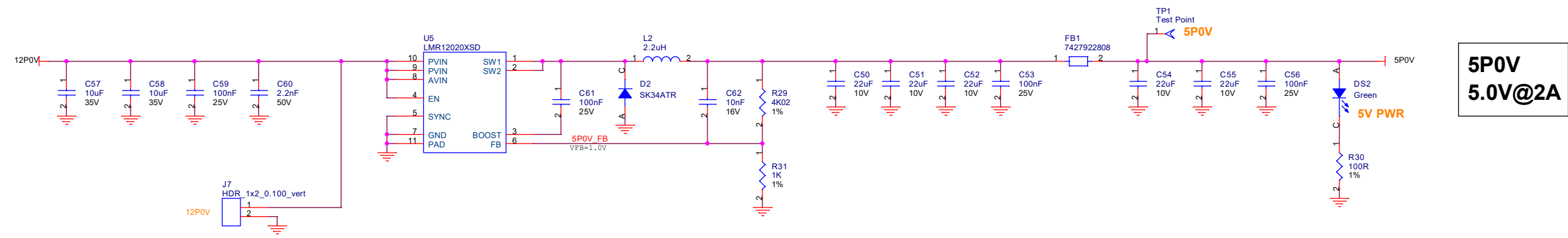


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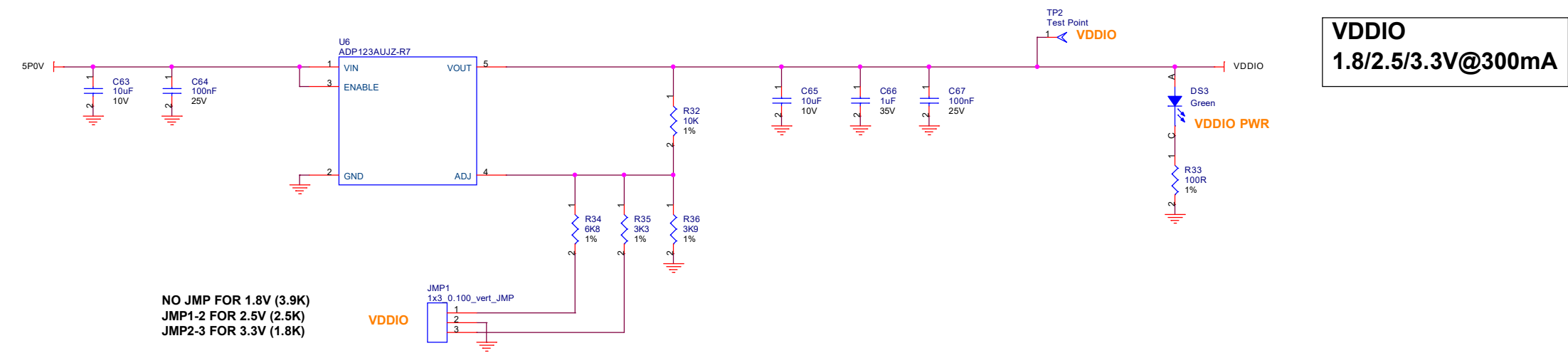
CKM Power Req	
IOVDD @ 20mA	
5P0V @ 50mA	

	Title	
	TangerineSDR DE Adapter Display & Jumpers	
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12P0V
11-15V@1A
POWER INPUT

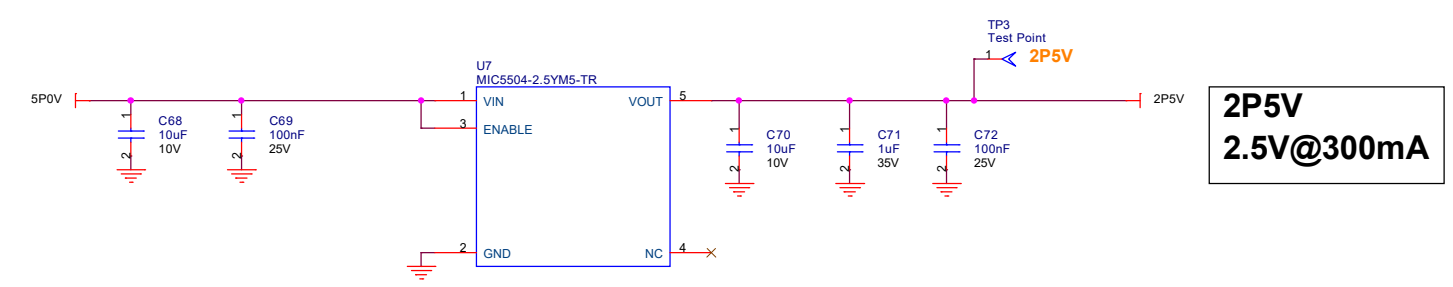


5P0V
5.0V@2A

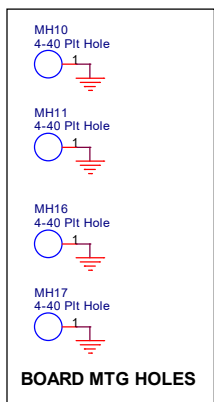


VDDIO
1.8/2.5/3.3V@300mA

NO JMP FOR 1.8V (3.9K)
 JMP1-2 FOR 2.5V (2.5K)
 JMP2-3 FOR 3.3V (1.8K)



2P5V
2.5V@300mA



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		Title TangerineSDR DE Adapter Power Supplies	
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