TSDR-RXM-5001D - TangerineSDR Dual Channel Receiver
Software Defined Radio.

Specifications available at: https://tangerinesdr.com

Requirements Document:
TSDR-RXM-5001D-REQ

Interface Control Document:
TSDR-RXM-5001D-ICD

Application Notes:
TSDR-RXM-5001D-APP_NOTES

Rev	Date	Name	Description
XA1	24Jan2020	N5EG	Initial, add directional arrows + clock select resistors.
XA2	27Jan2020	WA2DFI	Clean up, cosmetic changes only
XA3	28Jan2020	WA2DFI	Move 1.8V SPI pins to J1B, re-order 3.3V I2C pins on J1A
XA4	06Feb2020	D Baldwin	Udate properties on schematic
XA5	14Feb2020	WA2DFI	Correct libraries
XA6	14Feb2020	WA2DFI	Correct libraries correctly
XA7	18Feb2020	WA2DFI	Change connectors J4, J5, J6, J8, J10, J11, JP1, JP2. Added JP3 and JP4.
XA8	25Feb2020	WA2DFI	Pin swap
XA9	2 Mar2020	WA2DFI	Swap ins on JP2, fix DCO+ and DCO- labels
XA10	10Mar2020	WA2DFI	Fix DCO+ and DCO- labels
XA11	11Apr2020	WA2DFI	Swap OSC_CLK_INn and OSC_CLK_INp at J1 connector
XA12	17Apr2020	D Baldwin	Renumber.
XA13	28Apr2020	WA2DFI	Update revisions on sheets
XA14	24Aug2020	N5EG	Add jumper and build options tables to cover page
XA15	23Jun2021	WA2DFI	Fix I2C 1.8V interfaces, add translator to SYNC
XA16	11Jul2021	WA2DFI	Adjusted attenuator resistor values
XA17	14Jul2021	WA2DFI	Add bypass caps C90 & C91
XA18	14Jul2021	WA2DFI	Add bypass cap to VDDIO
XA19	14Jul2021	WA2DFI	Change note on P4
A	15Jul2021	WA2DFI	Release to A

Jumper Options

JP1	Channel 1 Receive Filter Bypass If Channel 1 does not have a receive filter installed, then insert the jumper to provide signal continuity around the missing filter.
JP2	Channel 2 Receive Filter Bypass If Channel 2 does not have a receive filter installed, then insert the jumper to provide signal continuity around the missing filter.
JP3	Channel 1 Receive Ground Bonding Install this jumper to bond the RF common connection of Channel 1 to the system ground if desired or if needed for other reasons.
JP4	Power to noise generator. If JP4 is not installed then all power is removed from the noise generator circuitry. Computer control of the noise generator is disabled. Install JP4 if you wish to be able to use the noise generator, and to turn it on and off under Computer control.
JP5	Channel 2 Receive Ground Bonding Install this jumper to bond the RF common connection of Channel 2 to the system ground if desired or if needed for other reasons.

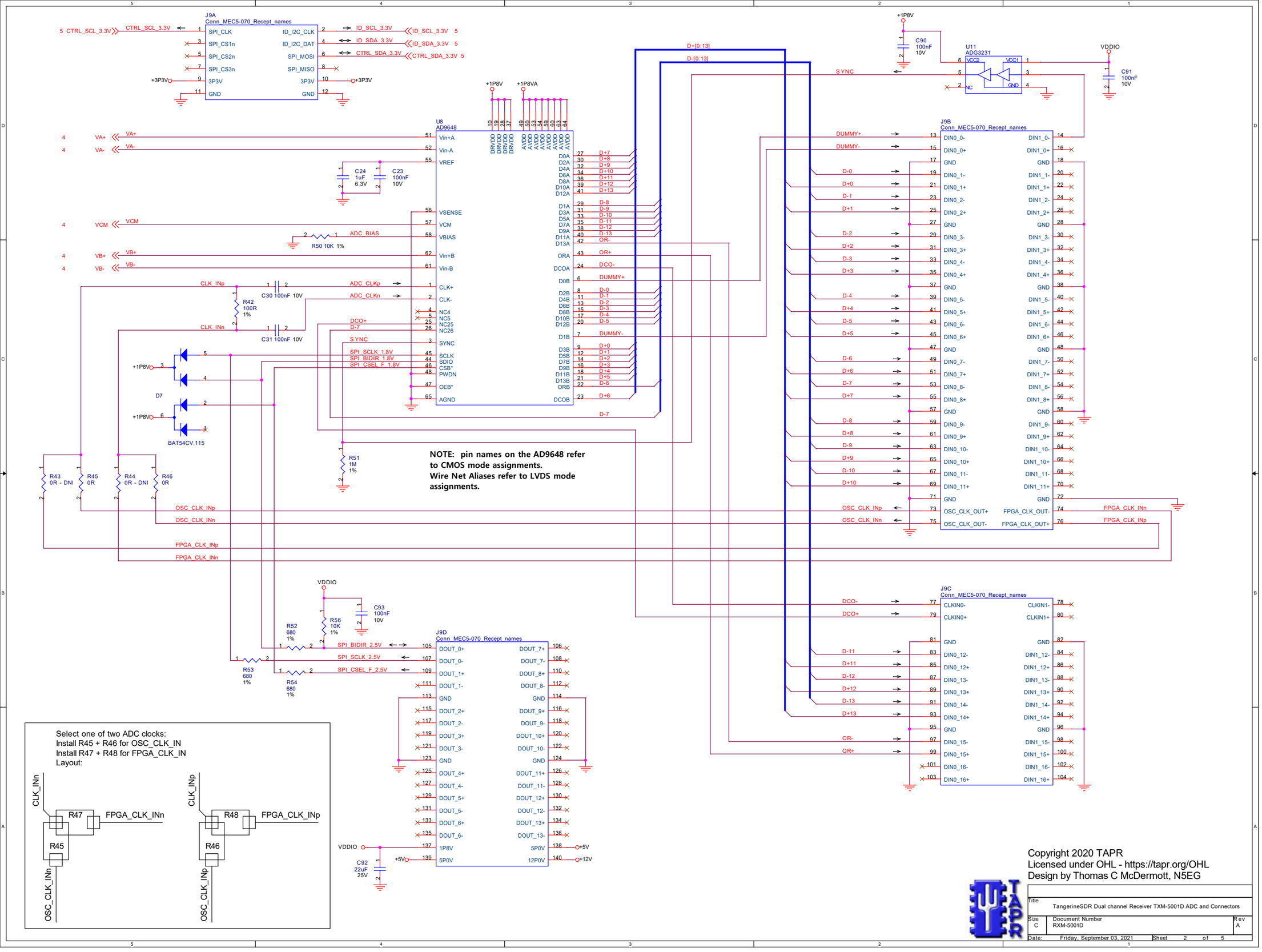
Build Options

Zero-ohm resistors R45 and R46 are installed by default. These route the clock from an external clock module through the MEC-140 connector to the ADC clock input (usually 122.88 MHz).

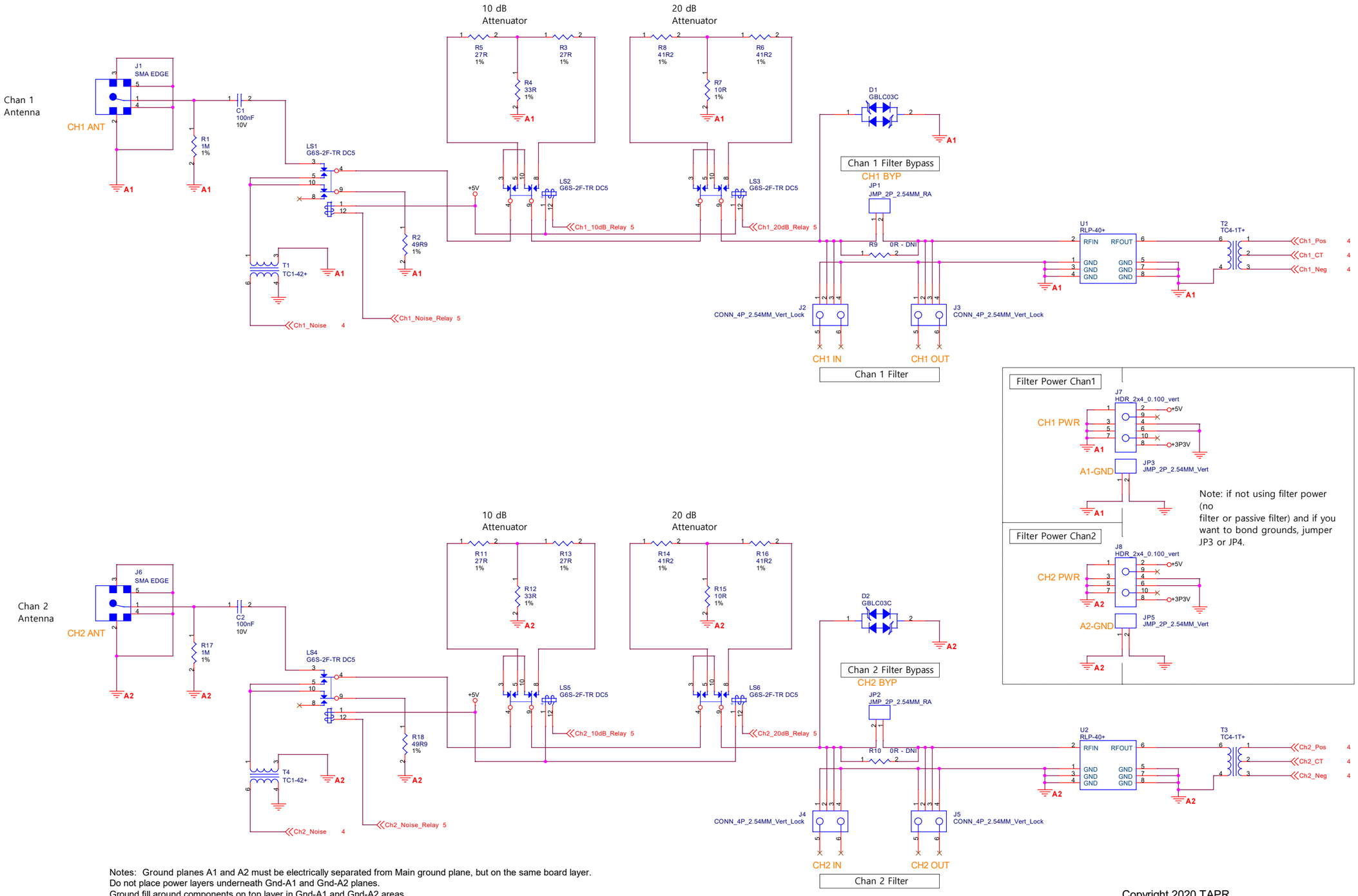
If an external clock module is not used, and instead the clock from the FPGA is used to clock the ADC, remove R45 and R46, and install zero-ohm resistors at R47 and R48. The FPGA clock will usually provide poorer clock / receiver performance than an external clock module.

Design by Thomas C McDermott, N5EG

Title	TangerineSDR Dual channel Receiver RXM-5001D Cover page	
Size C	Document Number RXM-5001D	Rev A
Date: Friday, September 03, 2021	Sheet 1 of 5	



Title	TangerineSDR Dual channel Receiver TXM-5001D ADC and Connectors	
Size C	Document Number RXM-5001D	Rev A
Date: Friday, September 03, 2021	Sheet 2 of 5	



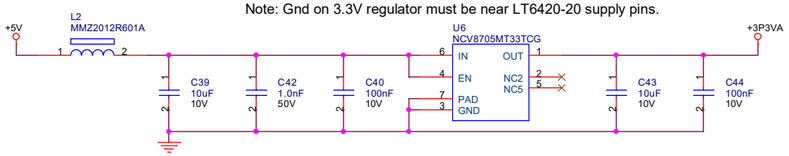
Notes: Ground planes A1 and A2 must be electrically separated from Main ground plane, but on the same board layer.
Do not place power layers underneath Gnd-A1 and Gnd-A2 planes.
Ground fill around components on top layer in Gnd-A1 and Gnd-A2 areas.
Relay coil pins only should be placed outside Gnd-A1 and Gnd-A2 plane areas.
Transformers should straddle the cut between their respective ground planes.

Gnd-A1, Gnd-A2, and Gnd are three separate ground planes.

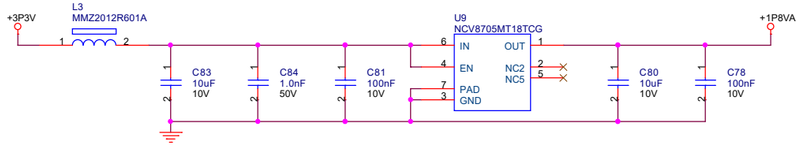
Design by Thomas C McDermott, N5EG

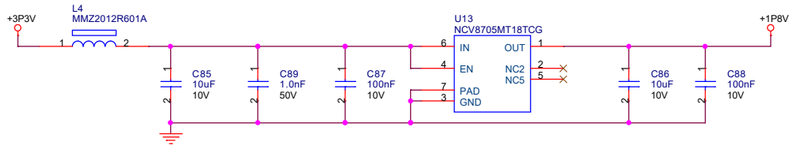
Title	TangerineSDR Dual channel Receiver RXM-5001D Filters	
Size C	Document Number RXM-5001D	Rev A
Date: Friday, September 03, 2021	Sheet 3 of 5	

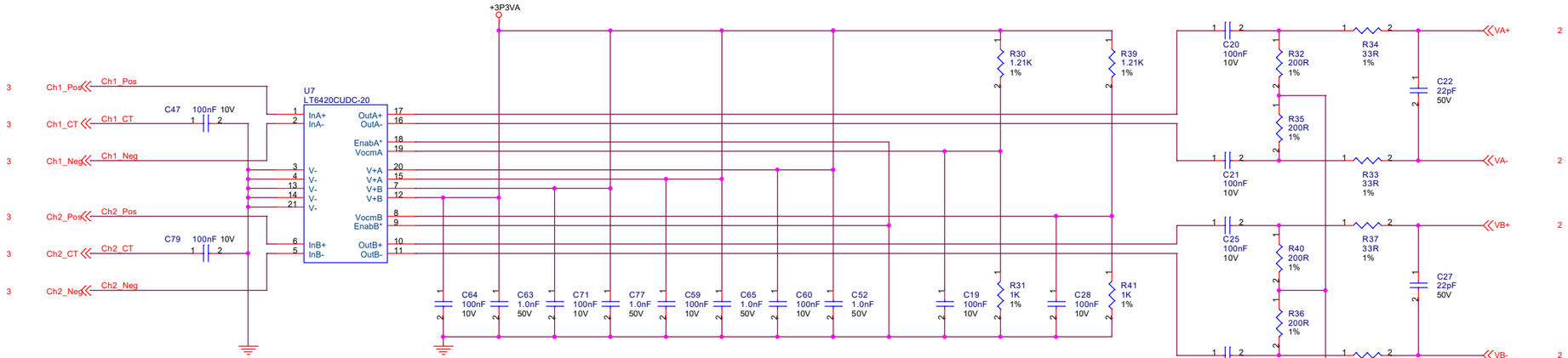
Note: Gnd on 3.3V regulator must be near LT6420-20 supply pins.



Note: Gnd on 1.8V regulator must be near AD9648 analog supply pins.

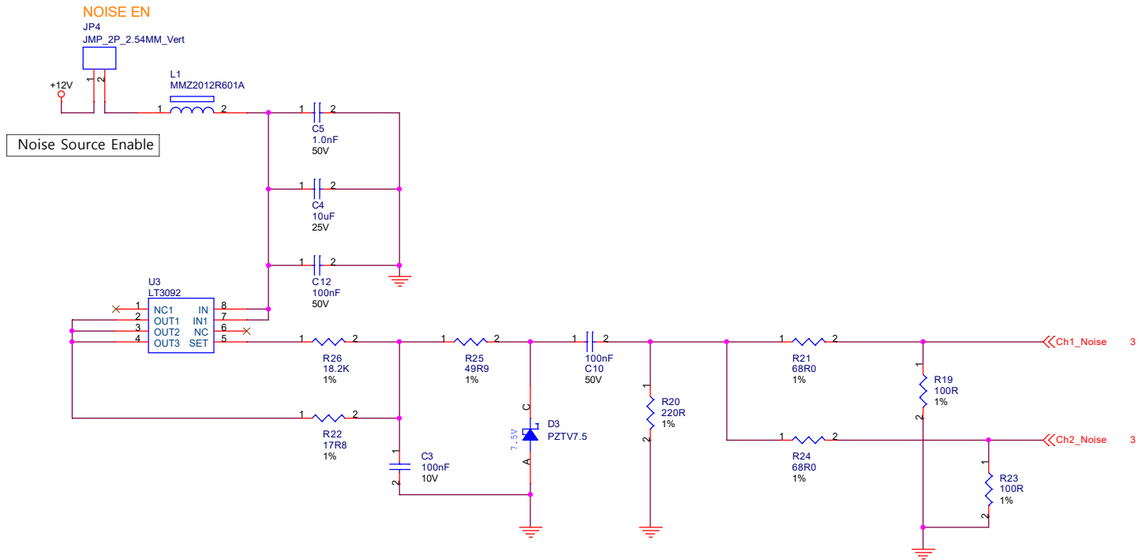






Note: 1 nF bypass caps must be extremely close to respective power pins.
100 nF bypass caps should be close to respective power pins.

NOISE EN



Note: Resistor values are set for 10 dB attenuation. Which is 15 dB ENR.

Design by Thomas C McDermott, N5EG

Title	TangerineSDR Dual channel Receiver RX-5001D LNA and Noise Source	
Size C	Document Number RXM-5001D	Rev A
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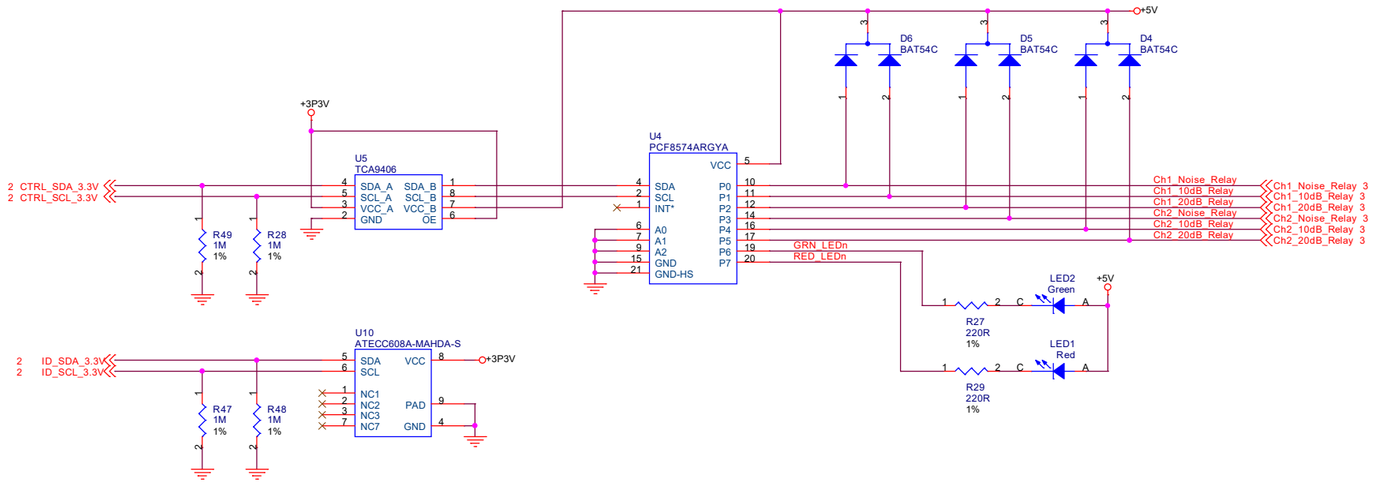
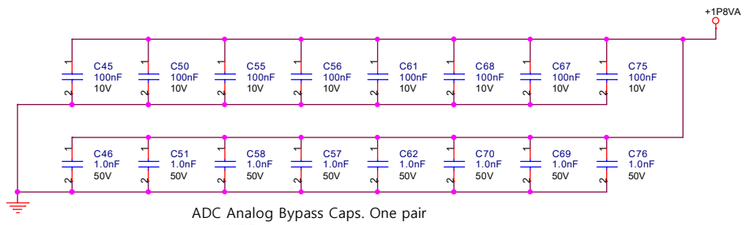
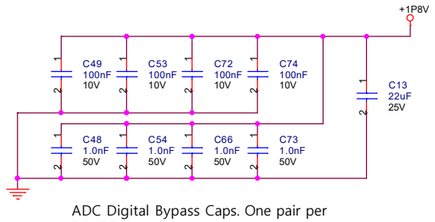
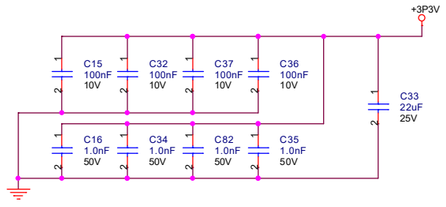
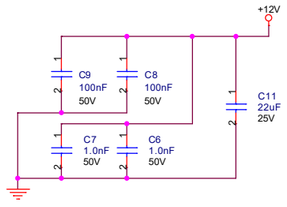


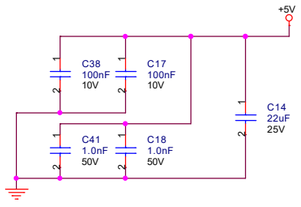


ADC Analog Bypass Caps. One pair per AVDD pin.









ADC Digital Bypass Caps. One pair per DRVDD pin.
Place all 22 uF bypass caps near board edge connector.

Design by Thomas C McDermott, N5EG

Title	TangerineSDR Dual channel Receiver RXM-5001D Bypass and Relay Ctl	
Size C	Document Number RXM-5001D	Rev A
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